

[Document Title](#)

**2M x 16 bit Pseudo SRAM Specification**

[Revision History](#)

Revision No.	History	Date	Remark
0.0	-. Initial Draft	May. 21 2008	Preliminary
0.1	Revised tBA (70ns to 25ns)	Jun. 11 2008	
1.0	-. EM7164SU16BLP, EM7164SU16BMP, EM7164SU16BNP, EM7164SU16BPP, EM7164SU16BRP & EM7164SU16BSP are unified to EM7164SU16BxP.  -. I <sub>CC1P</sub> changed to I <sub>CCP</sub> .  -. I <sub>CC1</sub> (Cycle time=Min.) changed to I <sub>CC2</sub> (Cycle time=Min.).  -. I <sub>CC1</sub> (Cycle time=1us) added to DC AND OPERATING CHARACTERISTICS table in page 5.	Dec. 15 2008	Release
1.1	-. Part name changed from EM7324SU16xP-70LF to EM7324SU16xP-70LFx  -. FEATURES & PRODUCT FAMILY updated in page 2.  -. ABSOLUTE MAXIMUM RATINGS table updated in page 4.  -. RECOMMENDED DC OPERATING CONDITIONS & DC AND OPERATING CHARACTERISTICS updated in page 5.  -. AC CHARACTERISTICS updated in page 6.  -. Note corrected in page 3 and 12.  -. PACKAGE DIMENSION modified in page 13.	Mar. 3 2009	

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### 2Mb x16 Pseudo Static RAM Specification

#### GENERAL DESCRIPTION

The EM7324SU16xP is 33,554,432 bits of Pseudo SRAM which uses DRAM type memory cells, but this device has refresh-free operation and extreme low power consumption technology. Furthermore the interface is compatible to a low power Asynchronous type SRAM. The EM7324SU16xP is organized as 2,097,152 Words x 16 bit.

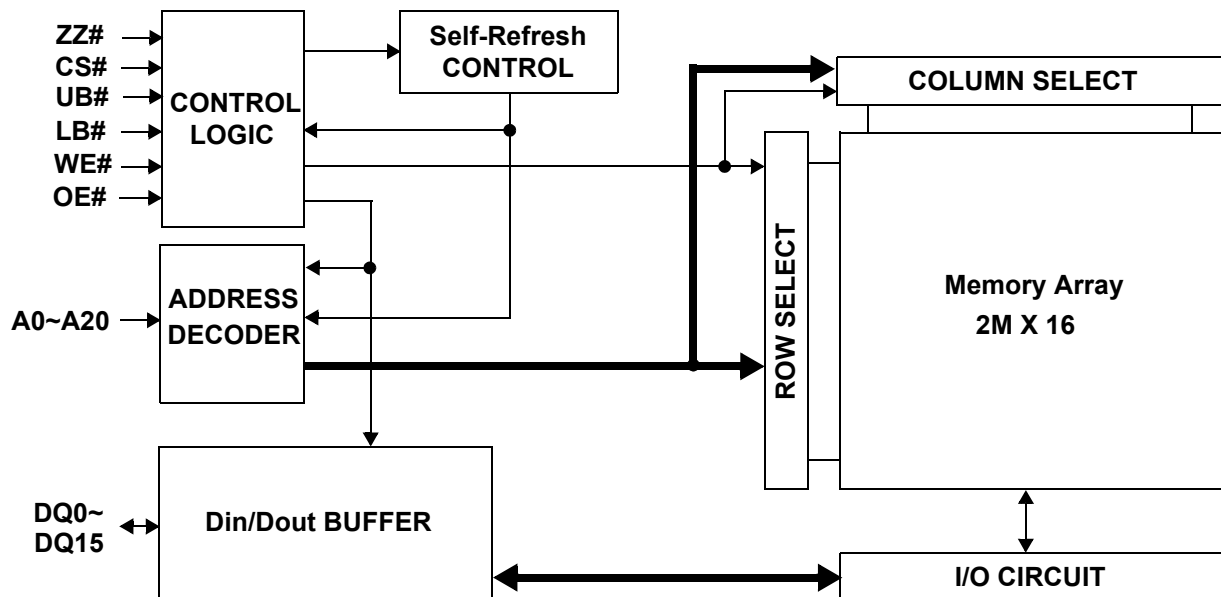
#### FEATURES

- Organization :2M x16
- Power Supply Voltage : 2.6 ~ 3.3V
- Separated I/O power(VccQ) & Core power(Vcc)
- Three state outputs
- Byte read/write control by UB# / LB#
- Auto-TCSR for power saving
- Package type : 48-FPBGA 6.0x7.0
- Operating Temperature
  - . Extended : -25°C ~ 85°C
  - . Wireless : -30°C ~ 85°C
  - . Industrial : -40°C ~ 85°C
- EM7324SU16LP support 8 page mode & DPD
- EM7324SU16MP support 8 page mode & Non-DPD
- EM7324SU16NP support 16 page mode & DPD
- EM7324SU16PP support 16 page mode & Non-DPD
- EM7324SU16RP support Non-page mode & DPD
- EM7324SU16SP support Non-page mode & Non-DPD

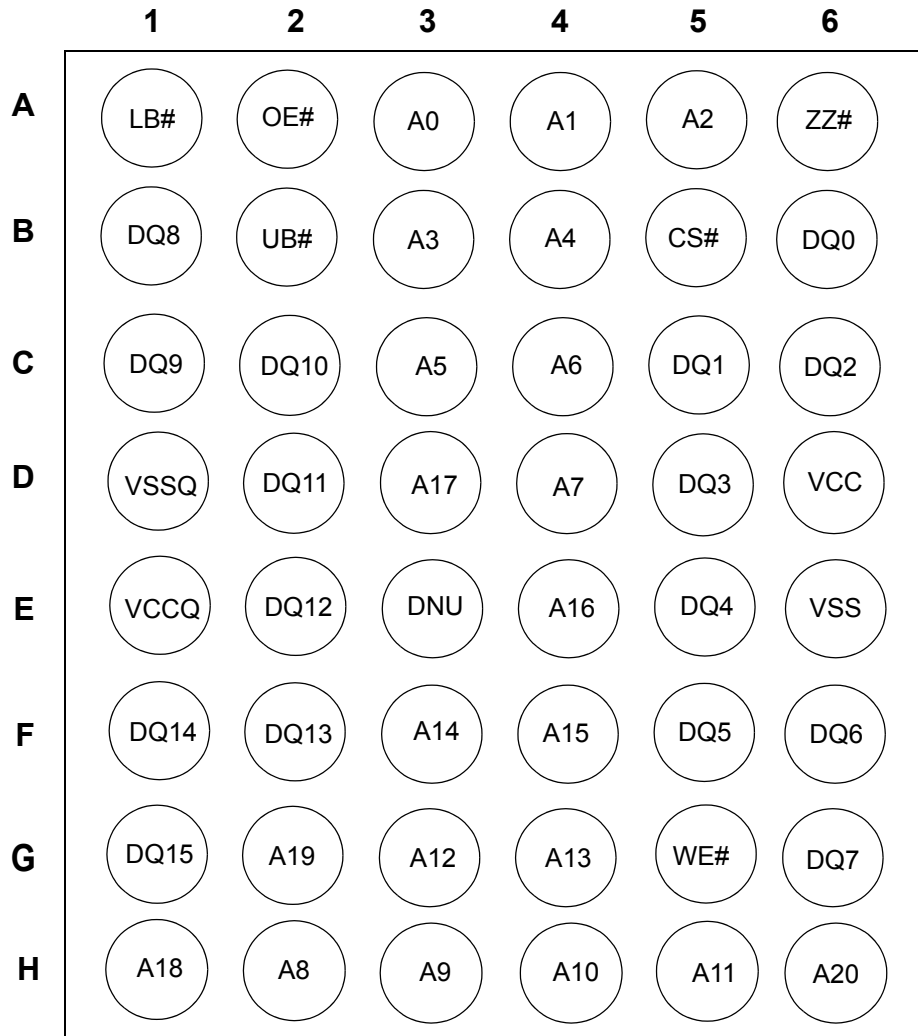
#### PRODUCT FAMILY

Part Number	Operating Temp.	Power Supply	Speed (t <sub>RC</sub> )	Power Dissipation		
				Standby (I <sub>SB</sub> , Max.)	Operating I <sub>CC</sub> ( Max.)	
					I <sub>CC1</sub> ( f = 1MHz)	I <sub>CC2</sub> ( f = f <sub>max</sub> )
EM7324SU16xP-70LF	-25°C to 85°C	2.6V to 3.3V	70ns	120uA	5mA	25mA
EM7324SU16xP-70LFW	-30°C to 85°C	2.6V to 3.3V	70ns	120uA	5mA	25mA
EM7324SU16xP-70LFI	-40°C to 85°C	2.6V to 3.3V	70ns	120uA	5mA	25mA

#### FUNCTION BLOCK DIAGRAM



**PIN DESCRIPTION ( 48-FBGA-6.00x7.00 )**



**TOP VIEW (Ball Down)**

Name	Function	Name	Function
CS#	Chip select input	LB#	Lower byte (DQ <sub>0~7</sub> )
OE#	Output enable input	UB#	Upper byte (DQ <sub>8~15</sub> )
WE#	Write enable input	VCC	Power supply
ZZ#	Low power control	VCCQ	I/O power supply
DQ <sub>0-15</sub>	Data in-out	VSS(Q)	Ground
A <sub>0-20</sub>	Address inputs	NC	No connection
DNU	Do not use		

Note : ZZ# pin is replaced to NC pin in EM7324SU16MP, EM7324SU16PP, EM7324SU16SP.

**ABSOLUTE MAXIMUM RATINGS <sup>1)</sup>**

Parameter		Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss		$V_{IN}, V_{OUT}$	-0.2 to $V_{CCQ}+0.3V$	V
Voltage on Vcc supply relative to Vss		$V_{CC}, V_{CCQ}$	-0.2 <sup>2)</sup> to 3.6V	V
Power Dissipation		$P_D$	1.0	W
Storage Temperature		$T_{STG}$	-65 to 150	°C
Operating Temperature	Extended	$T_A$	-25 to 85	°C
	Wireless		-30 to 85	°C
	Industrial		-40 to 85	°C

- Stresses greater than those listed above “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Undershoot at power-off : -1.0V in case of pulse width  $\leq 20ns$

**FUNCTIONAL DESCRIPTION**

CS#	ZZ#	OE#	WE#	LB#	UB#	DQ <sub>0~7</sub>	DQ <sub>8~15</sub>	Mode	Power
H	H	X	X	X	X	High-Z	High-Z	Deselected	Stand by
X	L	X	X	X	X	High-Z	High-Z	Deselected	Low Power Mode* <sup>2)</sup>
L	H	H	H	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Data Out	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Data Out	Upper Byte Read	Active
L	H	L	H	L	L	Data Out	Data Out	Word Read	Active
L	H	X	L	L	H	Data In	High-Z	Lower Byte Write	Active
L	H	X	L	H	L	High-Z	Data In	Upper Byte Write	Active
L	H	X	L	L	L	Data In	Data In	Word Write	Active

Note:

- X means don't care. (Must be low or high state)
- This Low Power mode is supported in EM7324SU16LP, EM7324SU16NP & EM7324SU16RP.

**RECOMMENDED DC OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	2.6	3.0	3.3	V
	V <sub>CCQ</sub>	2.6	3.0	3.3	V
Ground	V <sub>SS</sub> , V <sub>SSQ</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	0.8 * V <sub>CCQ</sub>	-	V <sub>CCQ</sub> + 0.2 <sup>1)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.2 <sup>2)</sup>	-	0.2 * V <sub>CCQ</sub>	V

1. Overshoot: V<sub>CC</sub> + 1.0 V in case of pulse width ≤ 20ns
2. Undershoot: -1.0 V in case of pulse width ≤ 20ns
3. Overshoot and undershoot are sampled, not 100% tested.

**CAPACITANCE<sup>1)</sup>** (f = 1MHz, T<sub>A</sub> = 25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> = 0V	-	8	pF

1. Capacitance is sampled, not 100% tested

**DC AND OPERATING CHARACTERISTICS**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CCQ</sub> , V <sub>CC</sub> = V <sub>CCmax</sub>	-1	-	1	uA
Output leakage current	I <sub>LO</sub>	CS# = V <sub>IH</sub> , ZZ# = V <sub>IH</sub> , OE# = V <sub>IH</sub> or WE# = V <sub>IL</sub> , V <sub>IO</sub> = V <sub>SS</sub> to V <sub>CCQ</sub> , V <sub>CC</sub> = V <sub>CCmax</sub>	-1	-	1	uA
Average operating current	I <sub>CC1</sub>	Cycle time = 1us, I <sub>IO</sub> = 0mA, 100% duty, CS# ≤ 0.2V, ZZ# ≥ V <sub>CCQ</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ V <sub>CCQ</sub> - 0.2V	-	-	5	mA
	I <sub>CC2</sub>	Cycle time = Min, I <sub>IO</sub> = 0mA, 100% duty, CS# = V <sub>IL</sub> , ZZ# = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	-	-	25	mA
Page access operating current	I <sub>CCP</sub>	t <sub>PC</sub> = Min, CS# = V <sub>IL</sub> , ZZ# = V <sub>IH</sub> , I <sub>IO</sub> = 0mA, Page add. cycling.	-	-	15	mA
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 0.5mA, V <sub>CC</sub> = V <sub>CCmin</sub>	-	-	0.2 * V <sub>CCQ</sub>	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -0.5mA, V <sub>CC</sub> = V <sub>CCmin</sub>	0.8 * V <sub>CCQ</sub>	-	-	V
Standby current (CMOS)	I <sub>SB</sub>	CS#, ZZ# ≥ V <sub>CCQ</sub> - 0.2V, Other inputs = 0 ~ V <sub>CCQ</sub> (Typ. condition : V <sub>CC</sub> = 3.0V @ 25°C) (Max. condition : V <sub>CC</sub> = 3.3V @ 85°C)	-	-	120	uA

1. Maximum I<sub>CC</sub> specifications are tested with V<sub>CC</sub> = V<sub>CCmax</sub>.

### AC OPERATING CONDITIONS

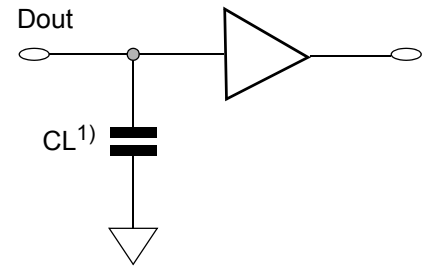
Test Conditions (Test Load and Test Input/Output Reference)

Input Pulse Level : 0.2V to  $V_{CCQ}-0.2V$

Input Rise and Fall Time : 5ns

Input and Output reference Voltage :  $V_{CCQ}/2$

Output Load (See right) :  $CL^{1)} = 30pF$



1. Including scope and Jig capacitance

### AC CHARACTERISTICS

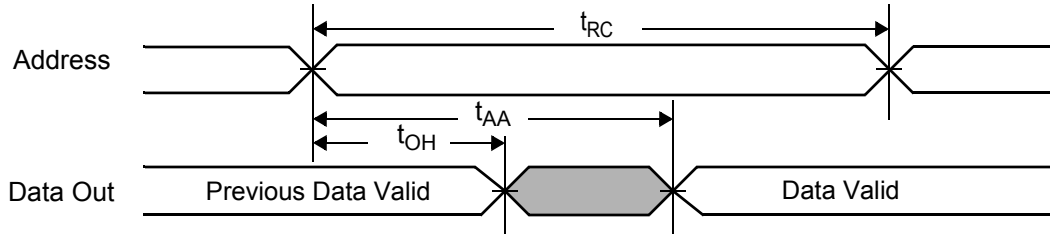
Parameter List		Symbol	Speed		Unit
			Min	Max	
Read	Read Cycle Time	$t_{RC}$	70	10k	ns
	Address access time	$t_{AA}$	-	70	ns
	Chip enable to data output	$t_{CO}$	-	70	ns
	Output enable to valid output	$t_{OE}$	-	25	ns
	UB#, LB# enable to data output	$t_{BA}$	-	25	ns
	Chip enable to low-Z output	$t_{LZ}$	10	-	ns
	UB#, LB# enable to low-Z output	$t_{BLZ}$	0	-	ns
	Output enable to low-Z output	$t_{OLZ}$	0	-	ns
	Chip disable to high-Z output	$t_{HZ}$	0	20	ns
	UB#, LB# disable to high-Z output	$t_{BHZ}$	0	20	ns
	Output disable to high-Z output	$t_{OHZ}$	0	20	ns
	Output hold from Address change	$t_{OH}$	5	-	ns
Write	Write Cycle Time	$t_{WC}$	70	10k	ns
	Chip enable to end of write	$t_{CW}$	60	-	ns
	Address setup time	$t_{AS}$	0	-	ns
	Address valid to end of write	$t_{AW}$	60	-	ns
	UB#, LB# valid to end of write	$t_{BW}$	60	-	ns
	Write pulse width	$t_{WP}$	50	-	ns
	Write recovery time	$t_{WR}$	0	-	ns
	Write to output high-Z	$t_{WHZ}$	0	20	ns
	Data to write time overlap	$t_{DW}$	20	-	ns
	Data hold from write time	$t_{DH}$	0	-	ns
	End write to output low-Z	$t_{OW}$	5	-	ns
Page	Maximum cycle time	$t_{MRC}^{*1)}$	-	10k	ns
	Page mode cycle time	$t_{PC}^{*1)}$	25	-	ns
	Page mode address access time	$t_{PAA}^{*1)}$	-	25	ns

#### NOTES

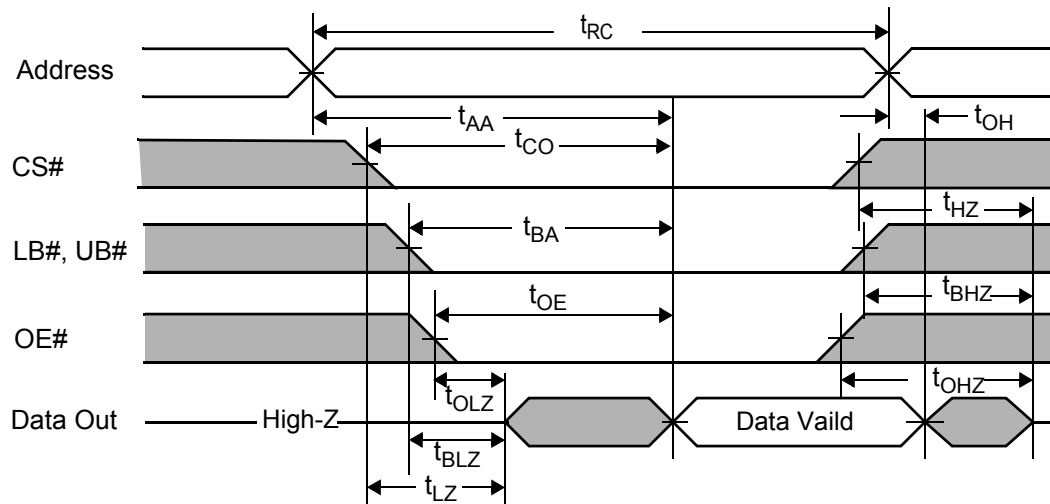
1. These parameters are not supported in EM7324SU16RP & EM7324SU16SP.

## TIMING DIAGRAMS

**READ CYCLE (1)** (Address controlled, CS#=OE#=V<sub>IL</sub>, ZZ#=WE#=V<sub>IH</sub>, UB# or/and LB#=V<sub>IL</sub>)



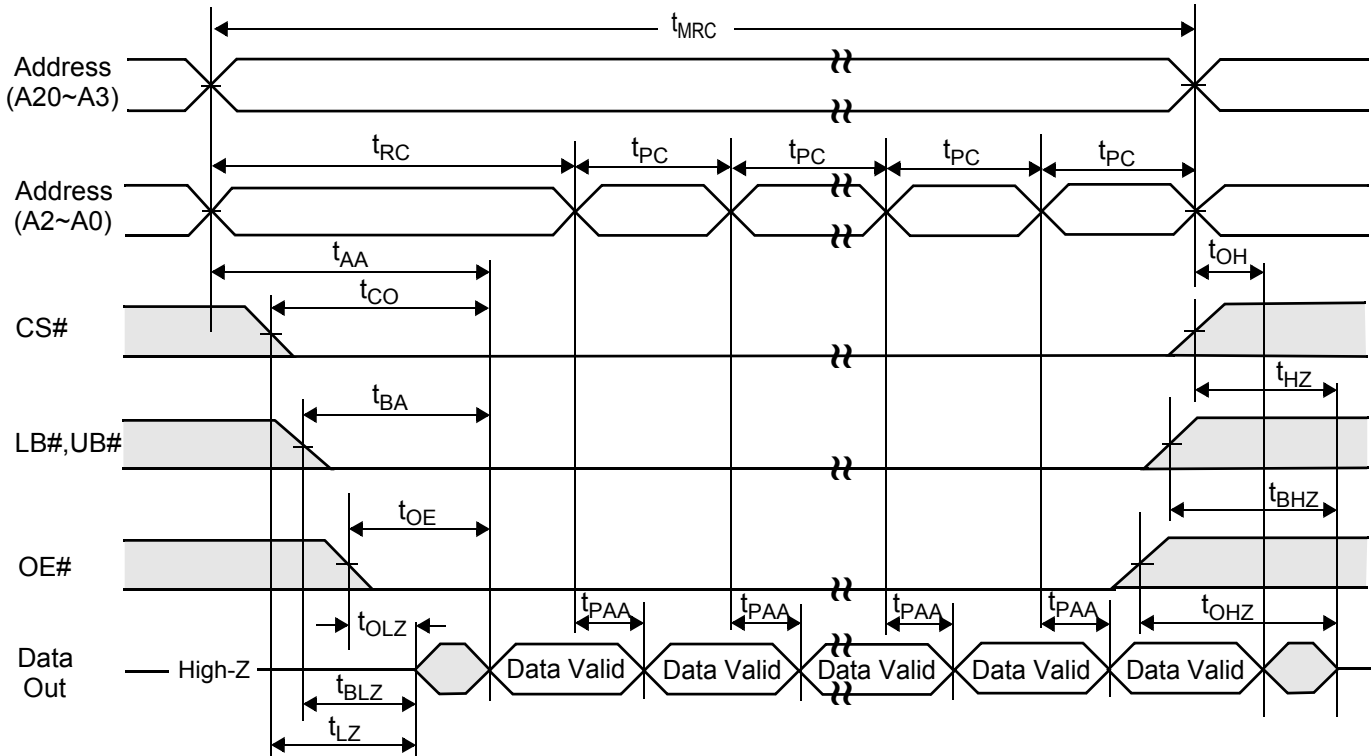
**READ CYCLE (2)** (ZZ#=WE#=V<sub>IH</sub>)



### NOTES (READ CYCLE)

1. t<sub>HZ</sub>, t<sub>BHZ</sub> and t<sub>OZH</sub> are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. Do not Access device with cycle timing shorter than t<sub>RC</sub> for continuous periods > 10us.

**PAGE READ CYCLE (1) (ZZ#=WE#=V<sub>IH</sub>, 8 Words access)**

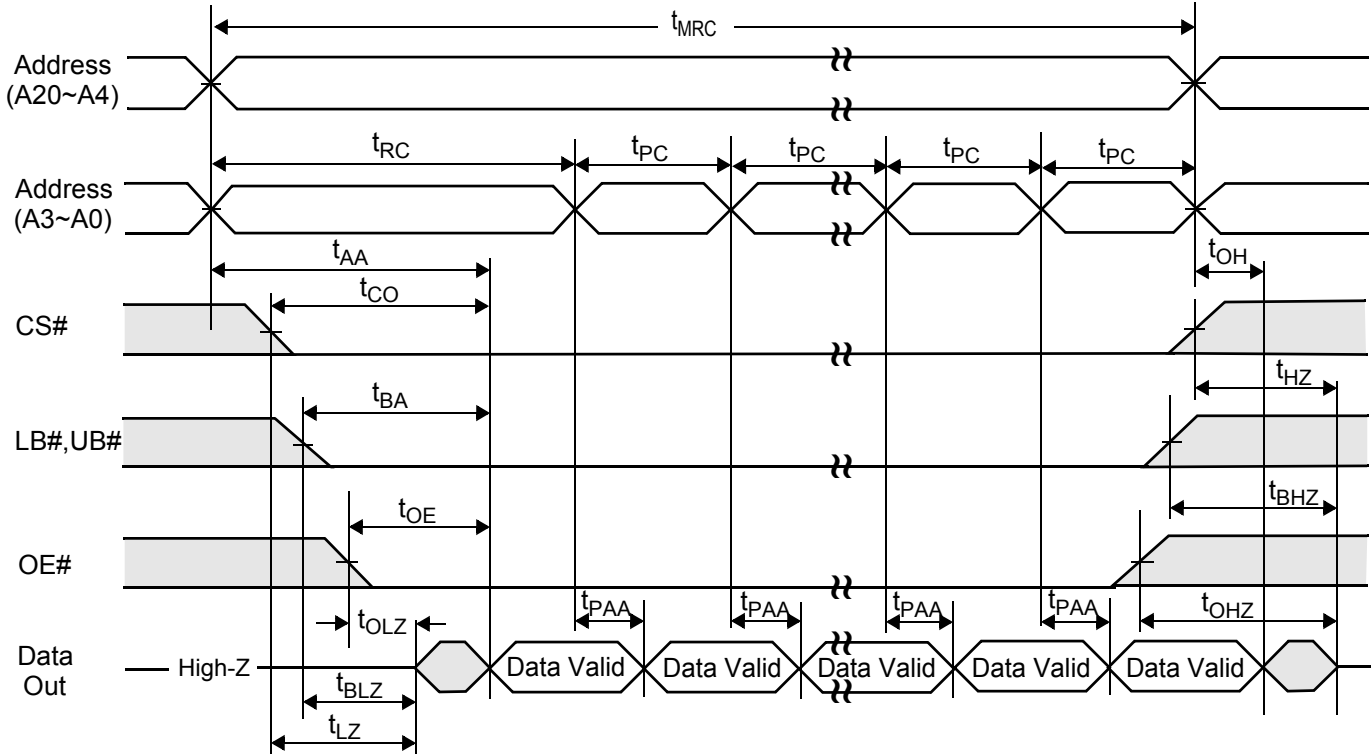


**NOTES (READ CYCLE)**

1.  $t_{HZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. Do not Access device with cycle timing shorter than  $t_{RC}$  for continuous periods > 10us.
3. This page read cycle(8 page mode) is supported in EM7324SU16LP & EM7324SU16MP.



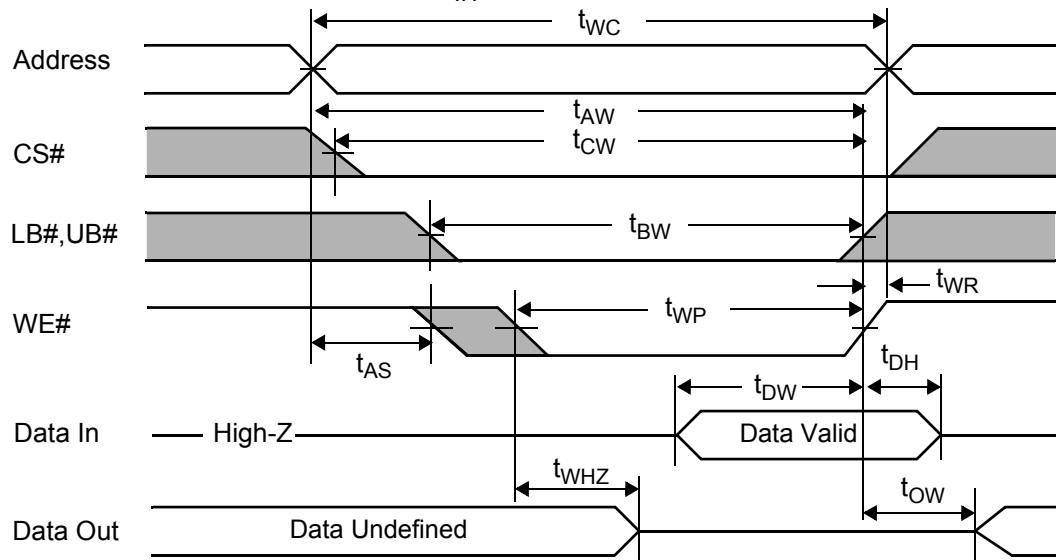
**PAGE READ CYCLE (2) (ZZ#=WE#=V<sub>IH</sub>, 16 Words access)**



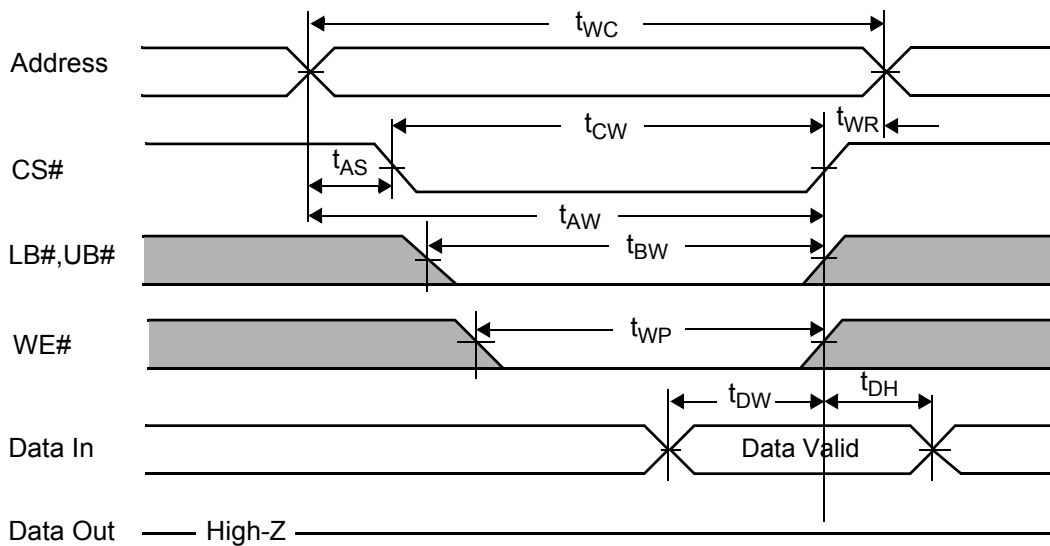
**NOTES (READ CYCLE)**

1.  $t_{HZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. Do not Access device with cycle timing shorter than  $t_{RC}$  for continuous periods > 10us.
3. This page read cycle(16 page mode) is supported in EM7324SU16NP & EM7324SU16PP.

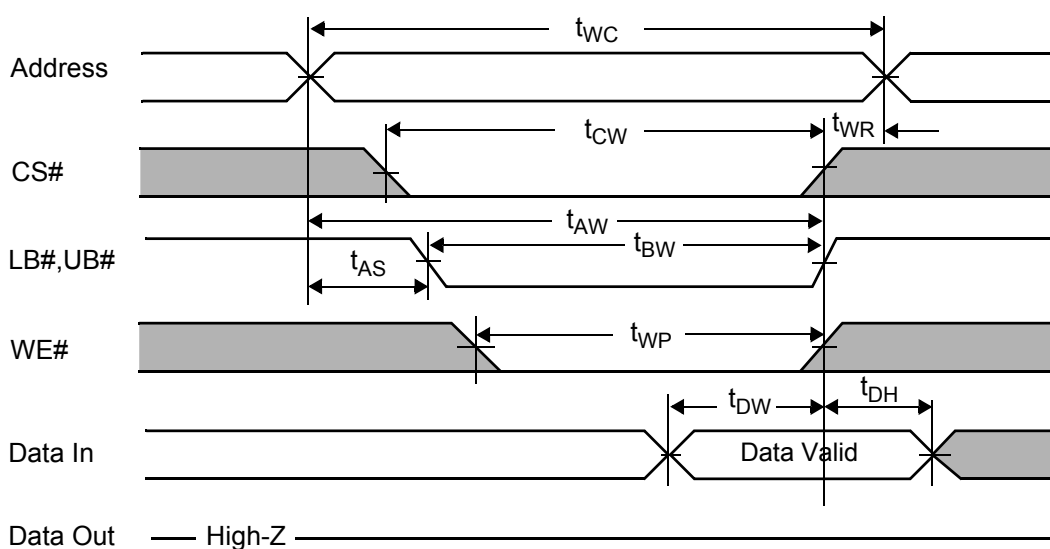
**WRITE CYCLE (1) (WE# controlled, ZZ#=V<sub>IH</sub>)**



**WRITE CYCLE (2) (CS# controlled, ZZ#=V<sub>IH</sub>)**



**WRITE CYCLE (3) (UB#/LB# controlled, ZZ#=V<sub>IH</sub>)**

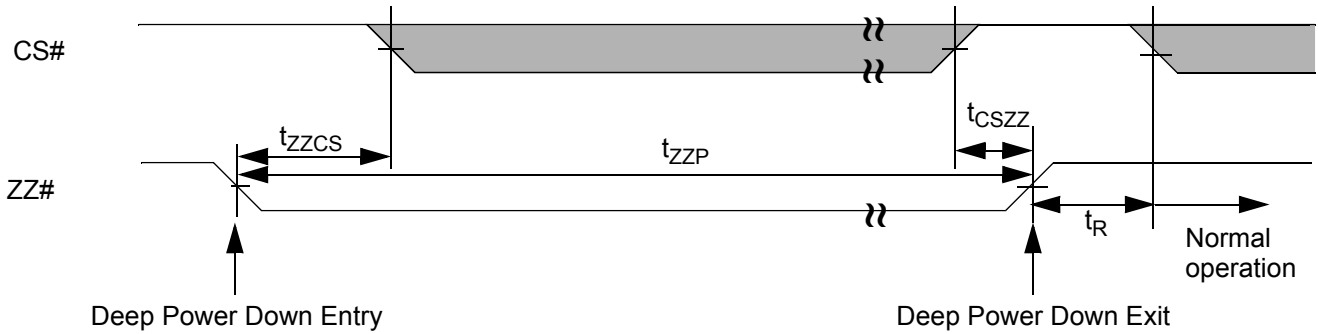


**NOTES (WRITE CYCLE)**

1. A write occurs during the overlap( $t_{WP}$ ) of low CS#, low WE# and low UB# or LB#. A write begins at the last transition among low CS# and low WE# with asserting UB# or LB# low for single byte operation or simultaneously asserting UB# and LB# low for word operation. A write ends at the earliest transition among high CS# and high WE#. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from CS# going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as CS# or WE# going high.
5. Do not access device with cycle timing shorter than  $t_{WC}$  for continuous periods > 10us.

**LOW POWER MODES**

**Deep Power Down Mode Entry/Exit**



**NOTES ( DEEP POWER DOWN )**

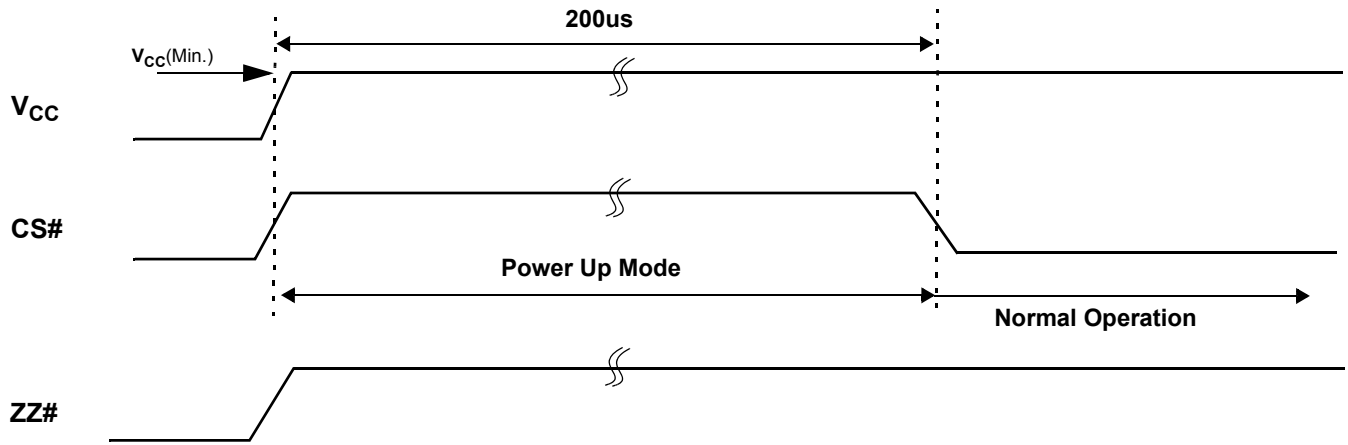
1. During Deep Power Down mode, all refresh related activity are disabled.
2. This DPD mode is supported in EM7324SU16LP, EM7324SU16NP & EM7324SU16RP.

Parameter	Description	Min.	Max.	Units
$t_{zzcs}$	ZZ# low to CS# low	0	-	ns
$t_{cszz}$	CS# high to ZZ# high	0	-	ns
$t_R$	Operation Recovery Time	200	-	us
$t_{zzp}$	ZZ# pulse width	20	-	ns

**Low Power Mode Characteristics**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Deep Power Down Current	$I_{ZZ}$	ZZ# $\leq$ 0.2V, Other inputs = 0 ~ $V_{CCQ}$ (Max. condition : $V_{CC}$ =3.3V @ 85°C)	-	-	10	uA

**TIMING WAVEFORM OF POWER UP**

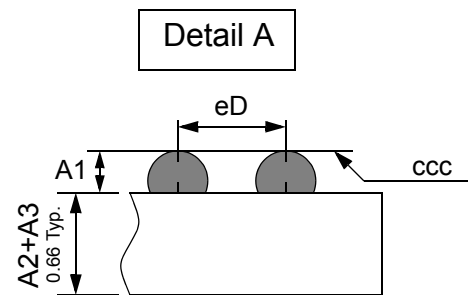
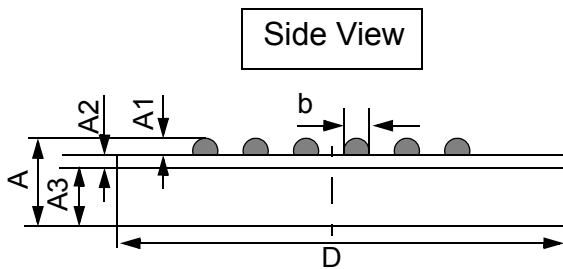
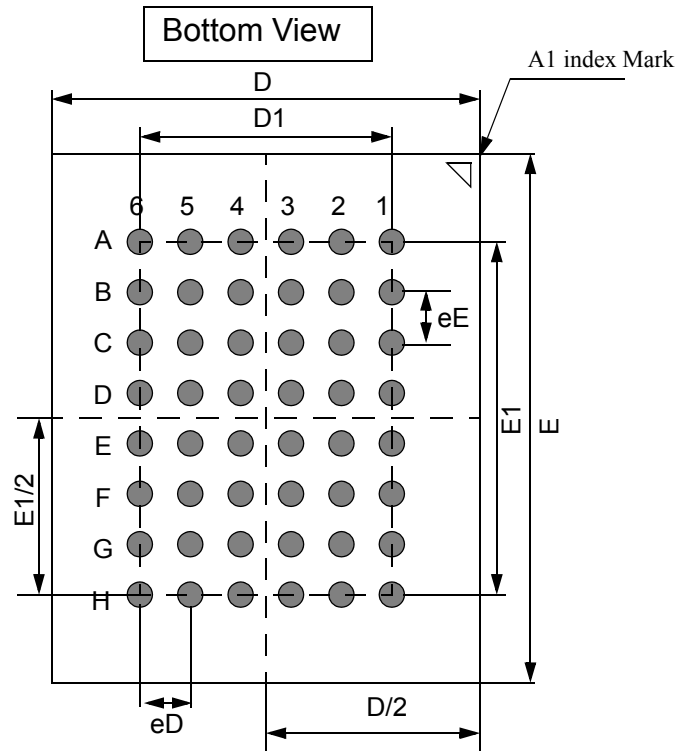
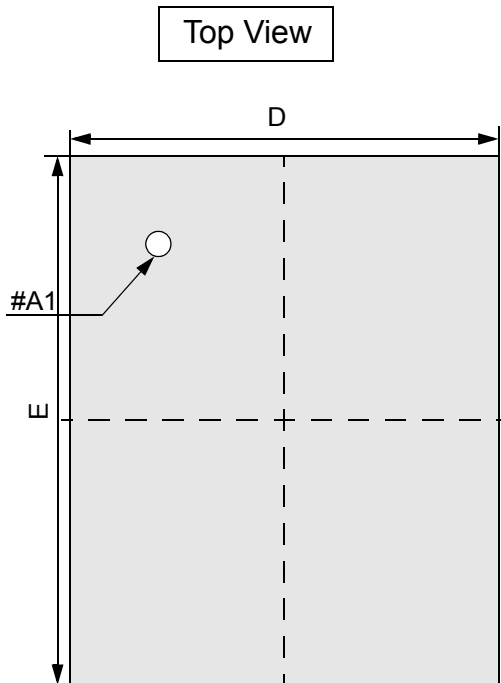


**NOTE ( POWER UP )**

1. After V<sub>CC</sub> reaches V<sub>CC(Min.)</sub> , wait 200us with CS# high. Then you get into the normal operation.
2. ZZ# pin is replaced to NC pin in EM7324SU16MP, EM7324SU16PP, EM7324SU16SP.

**PACKAGE DIMENSION**

48 Ball Fine Pitch BGA (0.75mm ball pitch)

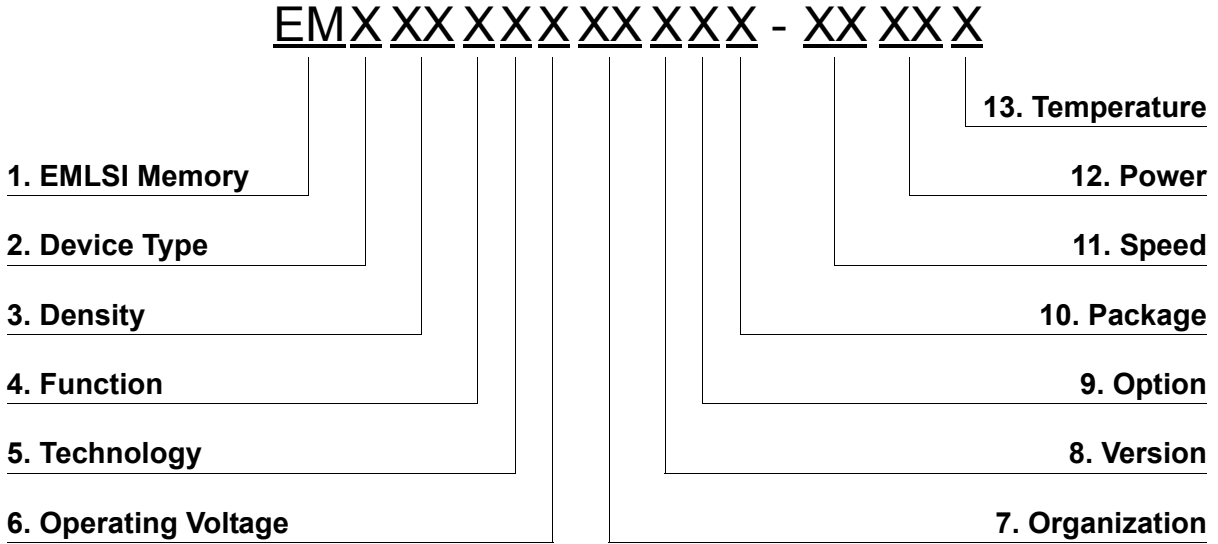


	Min	Typ	Max
A	-	-	1.00
A1	0.22	-	0.32
A2	-	0.21	-
A3	-	0.45	-
b	0.32	-	0.42
D	5.90	6.00	6.10
E	6.90	7.00	7.10
D1	-	3.75	-
E1	-	5.25	-
eE	-	0.75	-
eD	-	0.75	-
ccc	-	-	0.08

NOTES.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. ccc is coplanarity : 0.08(Max)

**MEMORY FUNCTION GUIDE**



- 1. Memory Component
- 2. Device Type
  - 6 ----- Low Power SRAM
  - 7 ----- STRAM
  - C ----- CellularRAM
- 3. Density
  - 4 ----- 4M
  - 8 ----- 8M
  - 16 ----- 16M
  - 32 ----- 32M
  - 64 ----- 64M
  - 28 ----- 128M
- 4. Function
  - 2 ----- Multiplexed async.
  - 3 ----- Multiplexed sync.
  - 4 ----- Demultiplexed async.
  - 5 ----- Multiplexed sync.
  - 6 ----- Demultiplexed sync.
- 5. Technology
  - S ----- Single Transistor
- 6. Operating Voltage
  - V ----- 3.3V
  - U ----- 3.0V
  - S ----- 2.5V
  - R ----- 2.0V
  - P ----- 1.8V
  - L ----- 1.5V
- 7. Organization
  - 8 ----- X8 bit
  - 16 ----- X16 bit
  - 32 ----- X32 bit
- 8. Version
  - Blank----- Mother die
  - A ----- 2 nd generation
  - B ----- 3 rd generation
  - C ----- 4 th generation
  - D ----- 5 th generation

- 9. Option
  - Blank----- No optional mode
  - J ----- Non-RBC
  - K ----- RBC
  - L ----- 8 page mode / DPD
  - M ----- 8 page mode / Non-DPD
  - N ----- 16 page mode / DPD
  - P ----- 16 page mode / Non-DPD
  - R ----- Non-page mode / DPD
  - S ----- Non-page mode / Non-DPD
- 10. Package
  - Blank----- Wafer
  - S ----- 32 sTSOP1
  - T ----- 32 TSOP1
  - U ----- 44 TSOP2
  - P ----- 48 FPBGA
  - Z ----- 52 FPBGA
  - Y ----- 54 FPBGA
  - W ----- 60 FPBGA
  - V ----- 90 FPBGA
- 11. Speed(@async.)
  - 45 ----- 45ns
  - 55 ----- 55ns
  - 60 ----- 60ns
  - 70 ----- 70ns
  - 85 ----- 85ns
  - 90 ----- 90ns
  - 10 ----- 100ns
  - 12 ----- 120ns
- 12. Power
  - LL ----- Low Low Power
  - LF ----- Low Low Power(Pb-free & Green)
  - L ----- Low Power
  - S ----- Standard Power
- 13. Temperature
  - Blank----- Extended (-25°C ~ 85°C)
  - W ----- Wireless (-30°C ~ 85°C)
  - I ----- Industrial (-40°C ~ 85°C)