1-Mbit (64K x 16) Static RAM

Features

- Temperature Ranges
  - — Industrial: –40°C to 85°C
  - — Automotive-A: –40°C to 85°C
  - — Automotive-E: –40°C to 125°C
- Pin-and function-compatible with CY7C1021CV33
- High speed
  - — t_{AA} = 10 ns
- Low active power
  - — I_{CC} = 60 mA @ 10 ns
- Low CMOS standby power
  - — I_{SB2} = 3 mA
- 2.0V data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Independent control of upper and lower bits
- Available in Pb-free 44-pin 400-Mil wide Molded SOJ, 44-pin TSOP II and 48-ball VFBGA packages

Functional Description[1]

The CY7C1021DV33 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O$_0$ through I/O$_7$), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O$_8$ through I/O$_{15}$) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O$_0$ to I/O$_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O$_8$ to I/O$_{15}$. See the truth table at the end of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O$_0$ through I/O$_{15}$) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the BHE and BLE are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1021DV33 is available in Pb-free 44-pin 400-Mil wide Molded SOJ, 44-pin TSOP II and 48-ball VFBGA packages.
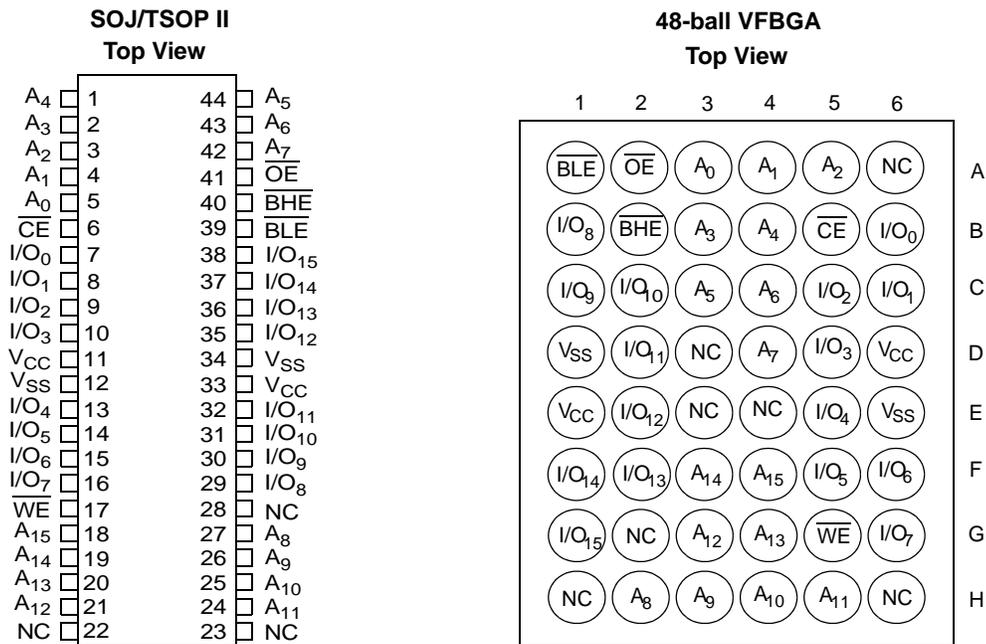
Logic Block Diagram
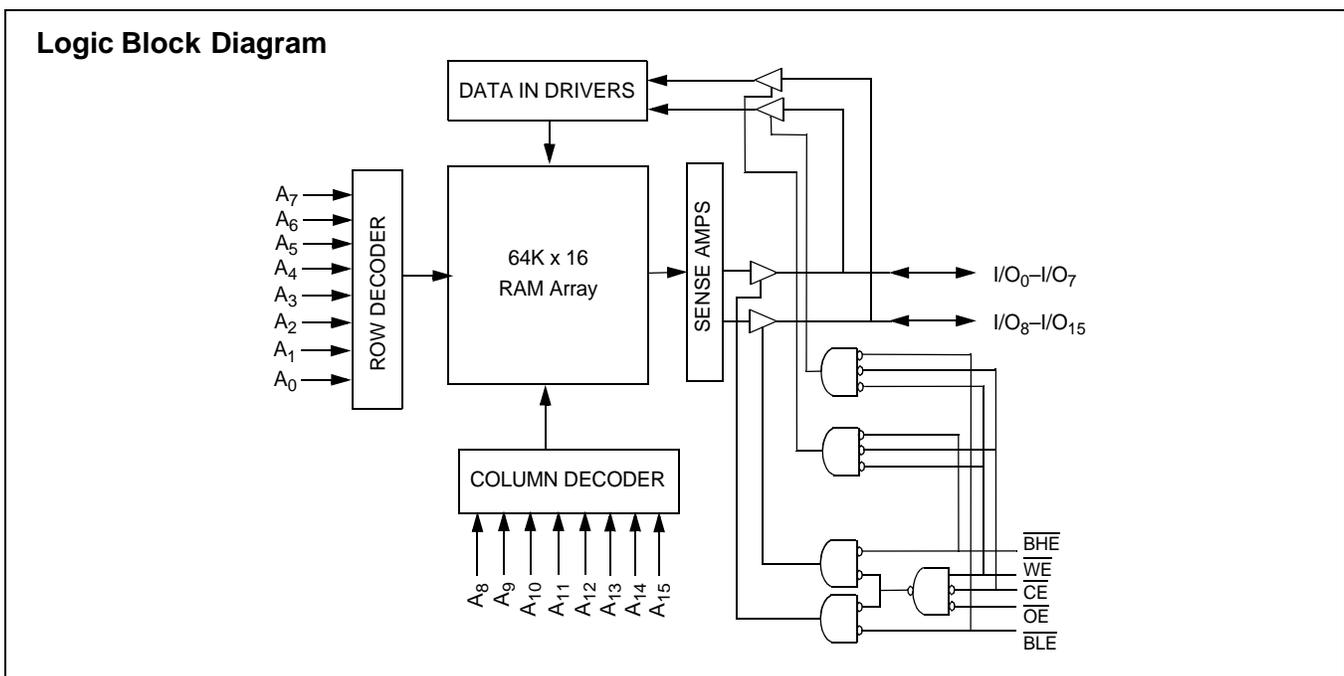
Note
1. For guidelines on SRAM system design, please refer to the "System Design Guidelines" Cypress application note, available on the internet at www.cypress.com

[+] Feedback

Selection Guide

	−10 (Industrial/Automotive-A)	−12 (Automotive-E)[2]	Unit
Maximum Access Time	10	12	ns
Maximum Operating Current	60	100	mA
Maximum CMOS Standby Current	3	15	mA

Pin Configuration[3]

SOJ/TSOP II
Top View

A_4	1	44	A_5
A_3	2	43	A_6
A_2	3	42	A_7
A_1	4	41	$\overline{OE}$
A_0	5	40	$\overline{BHE}$
$\overline{CE}$	6	39	$\overline{BLE}$
I/O_0	7	38	I/O_{15}
I/O_1	8	37	I/O_{14}
I/O_2	9	36	I/O_{13}
I/O_3	10	35	I/O_{12}
V_{CC}	11	34	V_{SS}
V_{SS}	12	33	V_{CC}
I/O_4	13	32	I/O_{11}
I/O_5	14	31	I/O_{10}
I/O_6	15	30	I/O_9
I/O_7	16	29	I/O_8
$\overline{WE}$	17	28	NC
A_{15}	18	27	A_8
A_{14}	19	26	A_9
A_{13}	20	25	A_{10}
A_{12}	21	24	A_{11}
NC	22	23	NC

48-ball VFBGA
Top View

	1	2	3	4	5	6	
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	NC	A
B	I/O_8	$\overline{BHE}$	A_3	A_4	$\overline{CE}$	I/O_0	B
C	I/O_9	I/O_{10}	A_5	A_6	I/O_2	I/O_1	C
D	V_{SS}	I/O_{11}	NC	A_7	I/O_3	V_{CC}	D
E	V_{CC}	I/O_{12}	NC	NC	I/O_4	V_{SS}	E
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6	F
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7	G
H	NC	A_8	A_9	A_{10}	A_{11}	NC	H

Notes
2. Automotive product information is Preliminary.
3. NC pins are not connected on the die.

[+] Feedback

Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature ....−65°C to +150°C

Ambient Temperature with
Power Applied..−55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[4] .... −0.3V to +4.6V

DC Voltage Applied to Outputs
in High-Z State[4] ....−0.3V to V_{CC}+0.3V

DC Input Voltage[4] ....−0.3V to V_{CC}+0.3V

Current into Outputs (LOW).. 20 mA

Static Discharge Voltage... > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	−40°C to +85°C	3.3V ± 0.3V	10 ns
Automotive-A	−40°C to +85°C		10 ns
Automotive-E	−40°C to +125°C		12 ns

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		−10 (Ind'l/Auto-A)		−12 (Auto-E)		Unit
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[4]			−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Leakage Current	GND $\leq V_I \leq V_{CC}$		−1	+1	−5	+5	μA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled		−1	+1	−5	+5	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{RC}	100 MHz		60		-	mA
			83 MHz		55		100	mA
			66 MHz		45		90	mA
			40 MHz		30		60	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}			10		50	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC}$ − 0.3V, $V_{IN} \geq V_{CC}$ − 0.3V or $V_{IN} \leq$ 0.3V, f = 0			3		15	mA

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance[5]

Parameter	Description	Test Conditions	SOJ	TSOP II	VFBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.52	53.91	36	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		36.75	21.24	9	°C/W

Notes
4. V_{IL} (min.) = −2.0V and V_{IH}(max) = V_{CC} + 1V for pulse durations of less than 5 ns.
5. Tested initially and after any design or process changes that may affect these parameters.

[+] Feedback

AC Test Loads and Waveforms[6]

OUTPUT O— Z = 50Ω

50Ω 30 pF*

1.5V O

* CAPACITIVE LOAD CONSISTS
OF ALL COMPONENTS OF THE
TEST ENVIRONMENT

(a)

3.0V

ALL INPUT PULSES

90%   90%

GND   10%   10%

Rise Time: 1 V/ns   Fall Time: 1 V/ns

(b)

High-Z characteristics: R 317Ω

3.3V O

OUTPUT O

5 pF   R2
351Ω

(c)
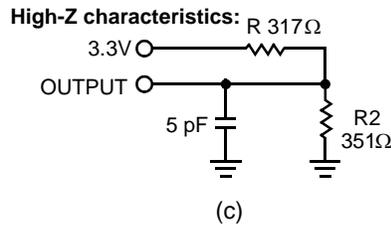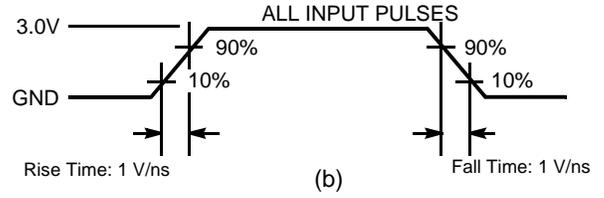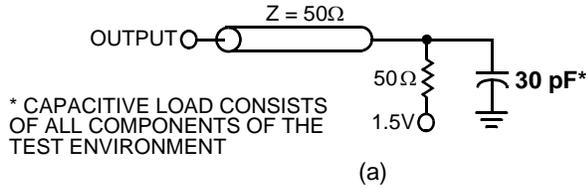
Note
6. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

Switching Characteristics Over the Operating Range[7]

| Parameter	Description	-10 (Ind'l/Auto-A)		-12 (Auto-E)		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{power}[8]	V_{CC}(typical) to the first access	100		100		μs
t_{RC}	Read Cycle Time	10		12		ns
t_{AA}	Address to Data Valid		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[10]	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[9, 10]		5		6	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[10]	3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[9, 10]		5		6	ns
t_{PU}[11]	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}[11]	$\overline{CE}$ HIGH to Power-Down		10		12	ns
t_{DBE}	Byte Enable to Data Valid		5		6	ns
t_{LZBE}	Byte Enable to Low-Z	0		0		ns
t_{HZBE}	Byte Disable to High-Z		6		6	ns
Write Cycle[12]						
t_{WC}	Write Cycle Time	10		12		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		9		ns
t_{AW}	Address Set-Up to Write End	8		9		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		ns
t_{SD}	Data Set-Up to Write End	5		6		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[10]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[9, 10]		5		6	ns
t_{BW}	Byte Enable to End of Write	7		8		ns

Notes
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
8. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
9. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in (c) of AC Test Loads. Transition is measured when the outputs enter a high impedance state
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
11. This parameter is guaranteed by design and is not tested.
12. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}/\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a Write and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

[+] Feedback

**Data Retention Characteristics** Over the Operating Range

Parameter	Description	Conditions		Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	Industrial		3	mA
			Automotive		15	mA
t_{CDR}[5]	Chip Deselect to Data Retention Time			0		ns
t_R[13]	Operation Recovery Time			t_{RC}		ns

Data Retention Waveform
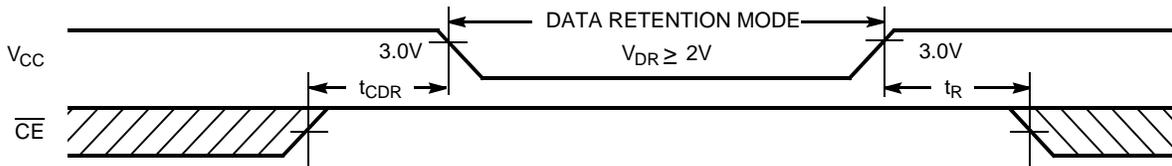
Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)[14, 15]
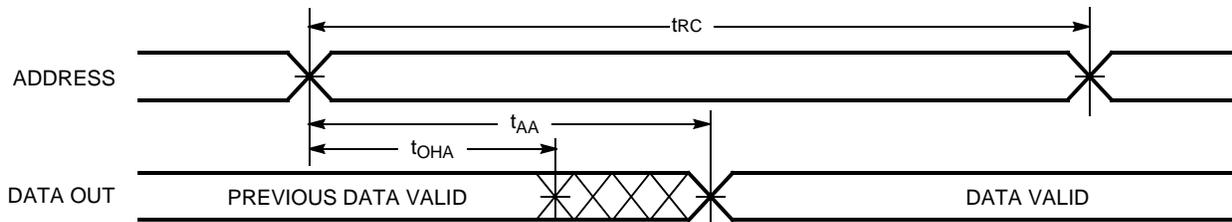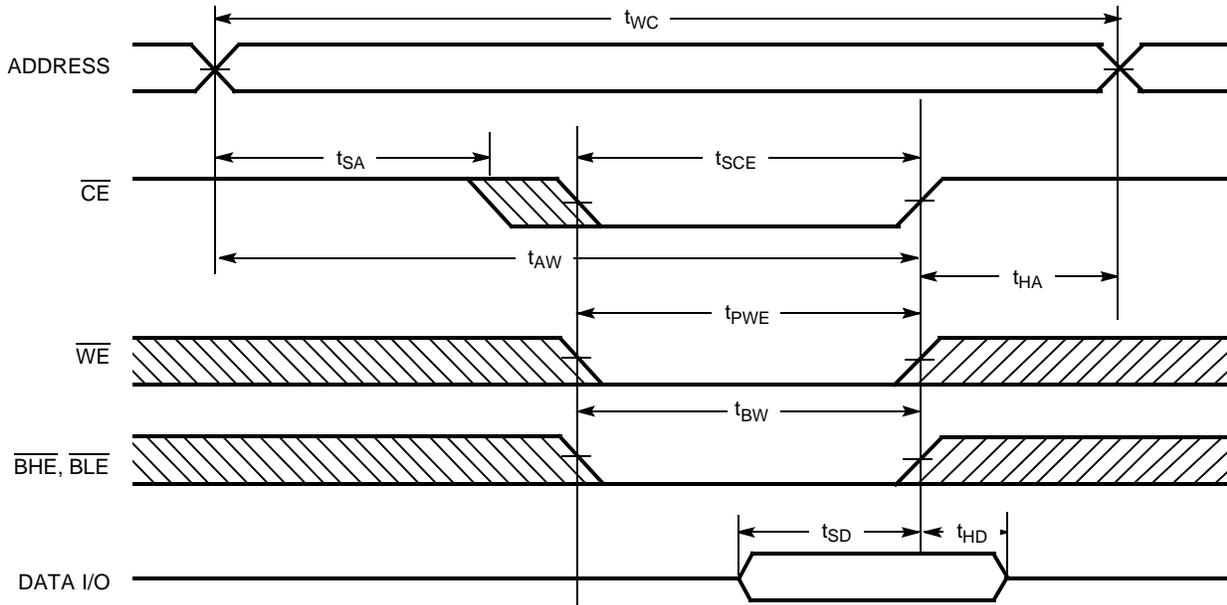

Read Cycle No. 2 (OE Controlled)[15, 16]
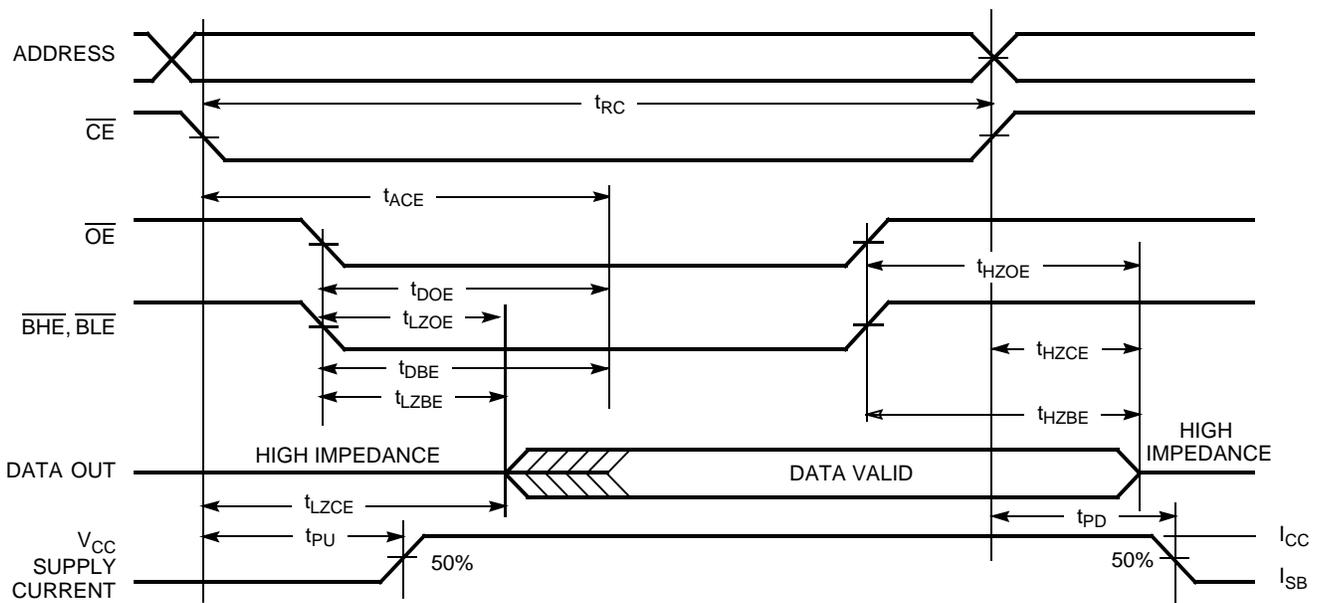
Notes
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50$ μs or stable at $V_{CC(min.)} \geq 50$ μs.
14. Device is continuously selected. OE, CE, BHE and/or BLE = V_{IL}.
15. WE is HIGH for Read cycle.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

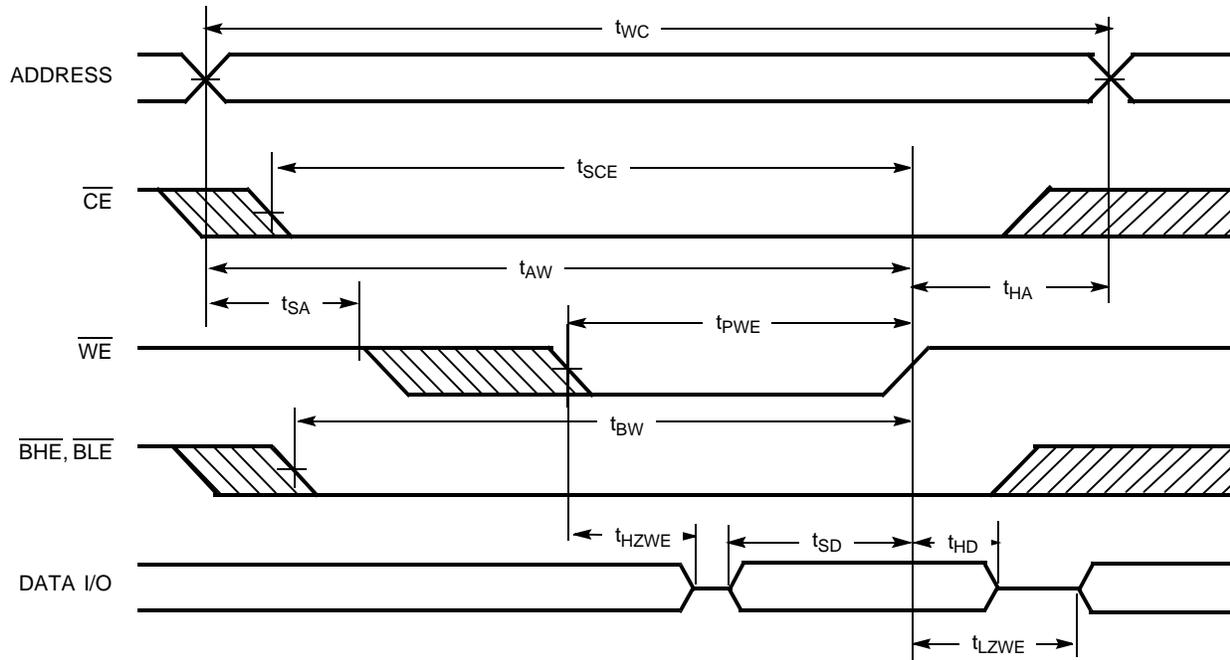**Write Cycle No. 1 ($\overline{CE}$ Controlled)**[17, 18]

Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)
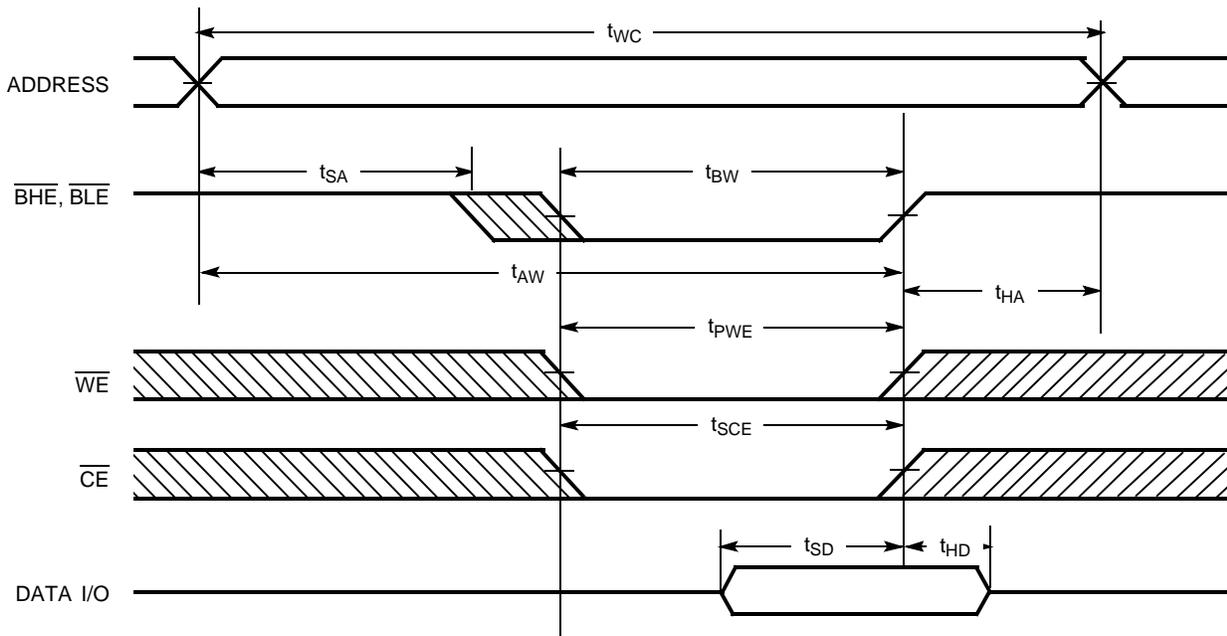
Notes
17. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IH}.
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High-Z	Read – Lower bits only	Active (I_{CC})
			H	L	High-Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High-Z	Write – Lower bits only	Active (I_{CC})
			H	L	High-Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1021DV33-10VXI	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1021DV33-10ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	
	CY7C1021DV33-10BVXI	51-85150	48-ball VFBGA (Pb-free)	
10	CY7C1021DV33-10ZSXA	51-85087	44-pin TSOP Type II (Pb-free)	Automotive-A
12	CY7C1021DV33-12ZSXE	51-85087	44-pin TSOP Type II (Pb-free)	Automotive-E

Please contact your local Cypress sales representative for availability of these parts.

[+] Feedback

Package Diagrams
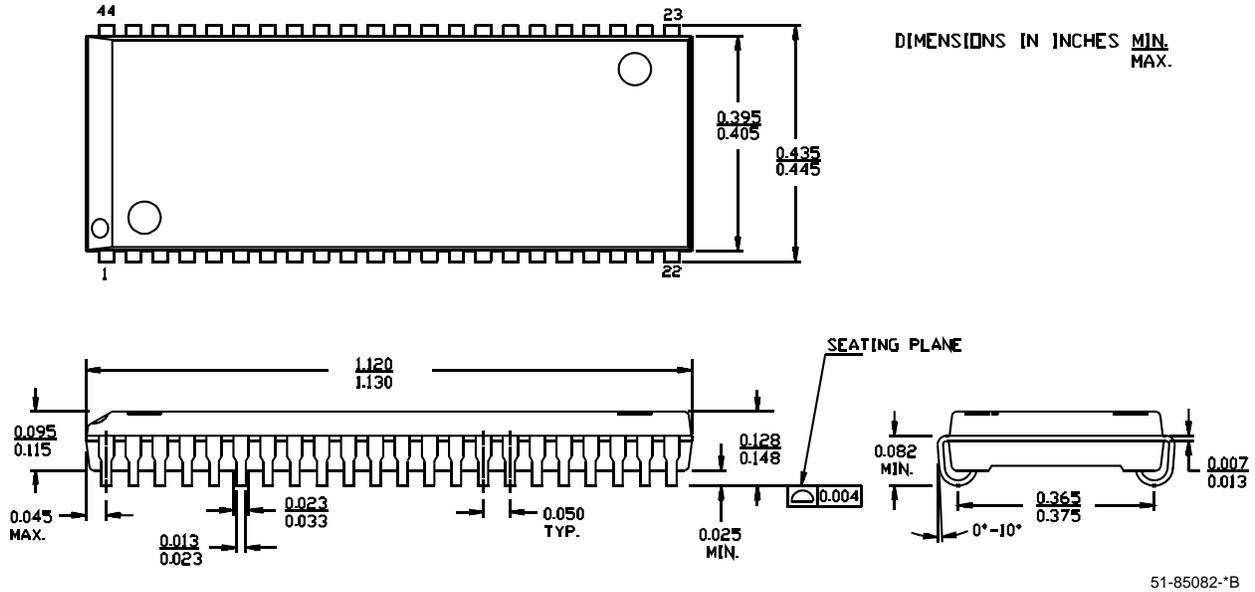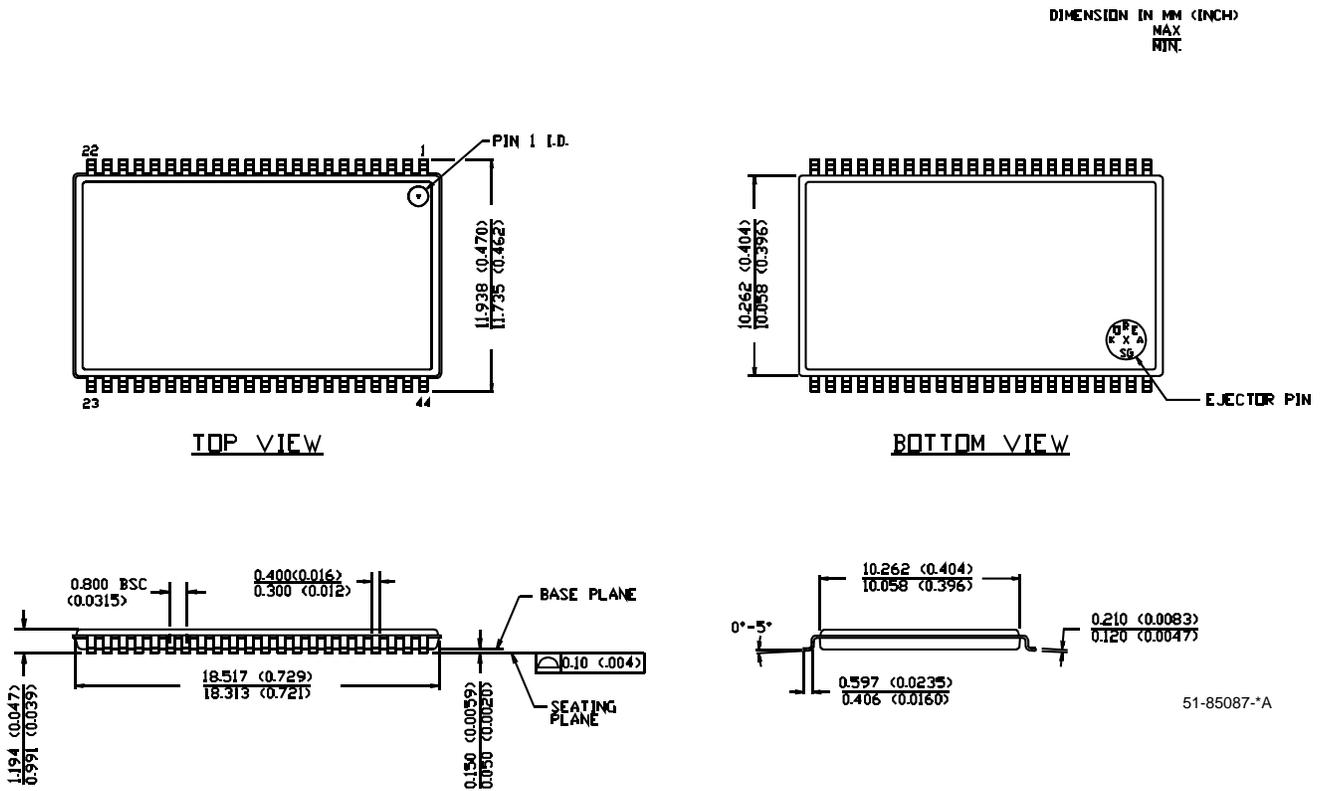
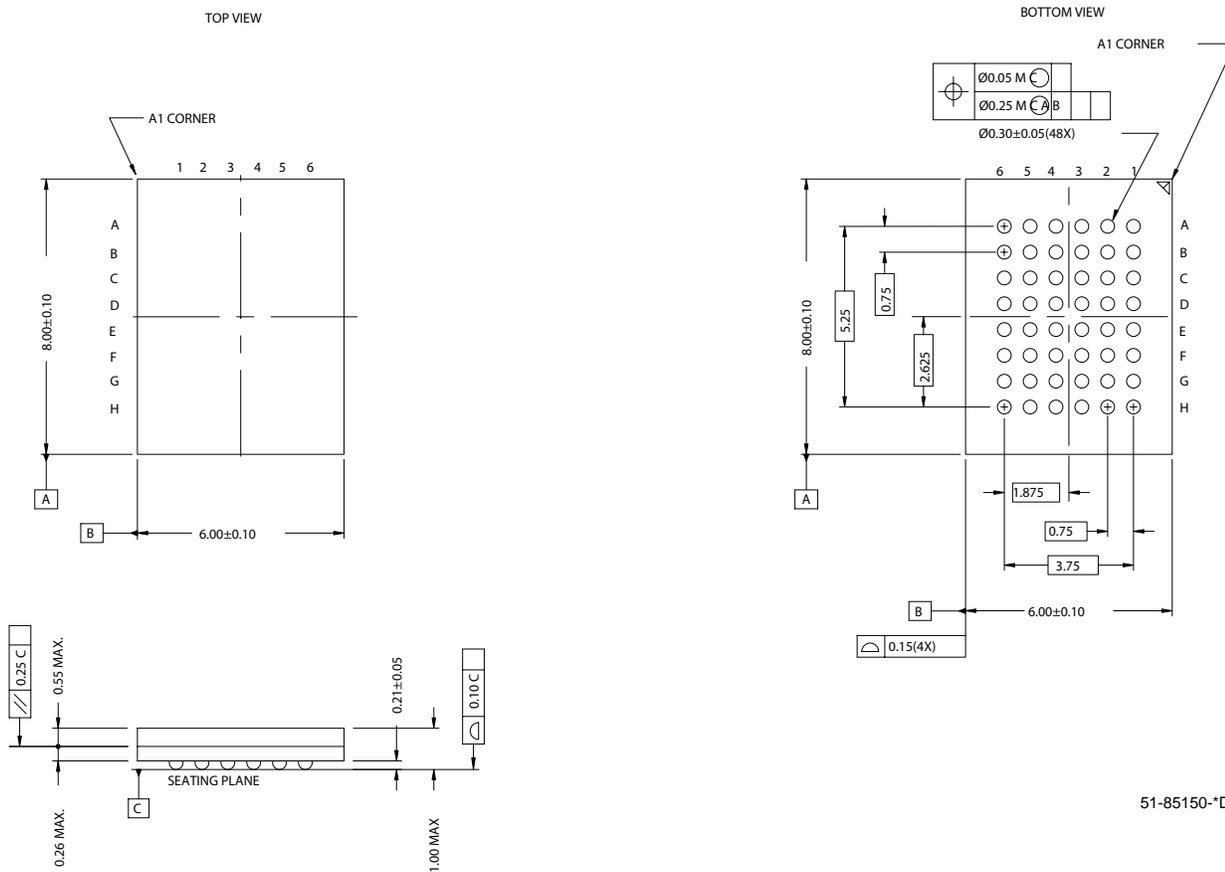**Figure 1. 44-pin (400-Mil) Molded SOJ (51-85082)**

51-85082-*B

Figure 2. 44-pin Thin Small Outline Package Type II (51-85087)

51-85087-*A

Package Diagrams (continued)

Figure 3. 48-ball VFBGA (6 x 8 x 1 mm) (51-85150)

TOP VIEW

BOTTOM VIEW

51-85150-*D

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[+] Feedback

Document History Page

Document Title: CY7C1021DV33, 1-Mbit (64K x 16) Static RAM				
Document Number: 38-05460				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233693	See ECN	RKF	DC parameters are modified as per Eros (Spec # 01-02165). Pb-free Offering In Ordering Information
*B	263769	See ECN	RKF	Changed I/O$_1$ – I/O$_{16}$ to I/O$_0$ – I/O$_{15}$ Added Data Retention Characteristics table Added T$_{power}$ Spec in Switching Characteristics table Shaded Ordering Information
*C	307601	See ECN	RKF	Reduced Speed bins to –8 and –10 ns
*D	520652	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 8 ns speed bin Added I$_{CC}$ values for the frequencies 83MHz, 66MHz and 40MHz Added Automotive Information Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V$_{CC}$+2V to V$_{CC}$+1V in footnote #4