12-Bit Deep Color with Quad HDMI Receiver

Data Sheet

ADV7614

FEATURES

- Ultralow jitter digital PLL
- 4:1 multiplexed HDMI receiver
  - HDMI 1.3a support
    - 36-/30-/24-bit deep color support
    - Flexible audio interface (DSD, DST, Dolby® TrueHD, DTS®-HD master audio, and DTS-HD high resolution audio)
  - 225 MHz HDMI receiver
  - HDMI repeater support
  - High-bandwidth digital content protection (HDCP 1.3)
  - Programmable/adaptive equalizer for cable lengths up to 30 meters
  - Internal EDID RAM
  - EDID with HDMI cable power support
  - CEC support
  - On-board audio mute controller
- General
  - Highly flexible output interface
  - 12-/10-/8-bit 4:4:4 or 12-/10-/8-bit 4:2:2 pixel output interface
  - STDI function support standard identification
  - Any-to-any 3 × 3 color space conversion matrixes
  - Free-run time generator
  - 2 programmable interrupt request output pins
  - Color controls
- Low standby power

APPLICATIONS

- Advanced TVs
  - AVR video receivers
  - PDP HDTVs
  - LCD TVs (HDTV ready)
  - OLED HDTVs
- LCD/DLP front projectors
- HDMI switchers

GENERAL DESCRIPTION

The ADV7614 is a high quality, single-chip integrated 4:1 multiplexed High-Definition Multimedia Interface (HDMI®) receiver.

The ADV7614 incorporates a quad input HDMI receiver that supports all HDTV formats up to 1080p and displays resolutions up to UXGA (1600 × 1200 at 60 Hz). The reception of encrypted video is possible with the inclusion of HDCP. The HDMI receiver also includes programmable/adaptive equalization that ensures robust operation of the interface with cable lengths up to 30 meters.

The ADV7614 provides complete audio support for eight channels of I²S audio, Sony/Philips digital interface format (S/PDIF) digital audio output, and super audio CD (SACD) and compressed SACD support with direct stream digital (DSD) and direct stream transfer (DST) output interfaces, respectively. The HDMI receiver also supports high bit rate (HBR) audio streaming to allow recovery (and downstream processing) of compressed lossless audio formats, including Dolby® TrueHD and DTS®-HD master audio or DTS-HD high resolution audio. In addition, it also provides an advanced audio functionality, such as a mute controller that prevents audible extraneous noise in the audio output.

Fabricated in an advanced CMOS process, the ADV7614 is provided in a space-saving, 260-ball 15 mm × 15 mm CSP_BGA surface-mount, RoHS-compliant package. The ADV7614 is specified over the −40°C to +70°C temperature range.

Advantiv® Advanced Television Solutions by Analog Devices | NSV® Precision Video by Analog Devices

Rev. C

Document Feedback

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REVISION HISTORY

9/13—Revision C: Initial Version

FUNCTIONAL BLOCK DIAGRAM

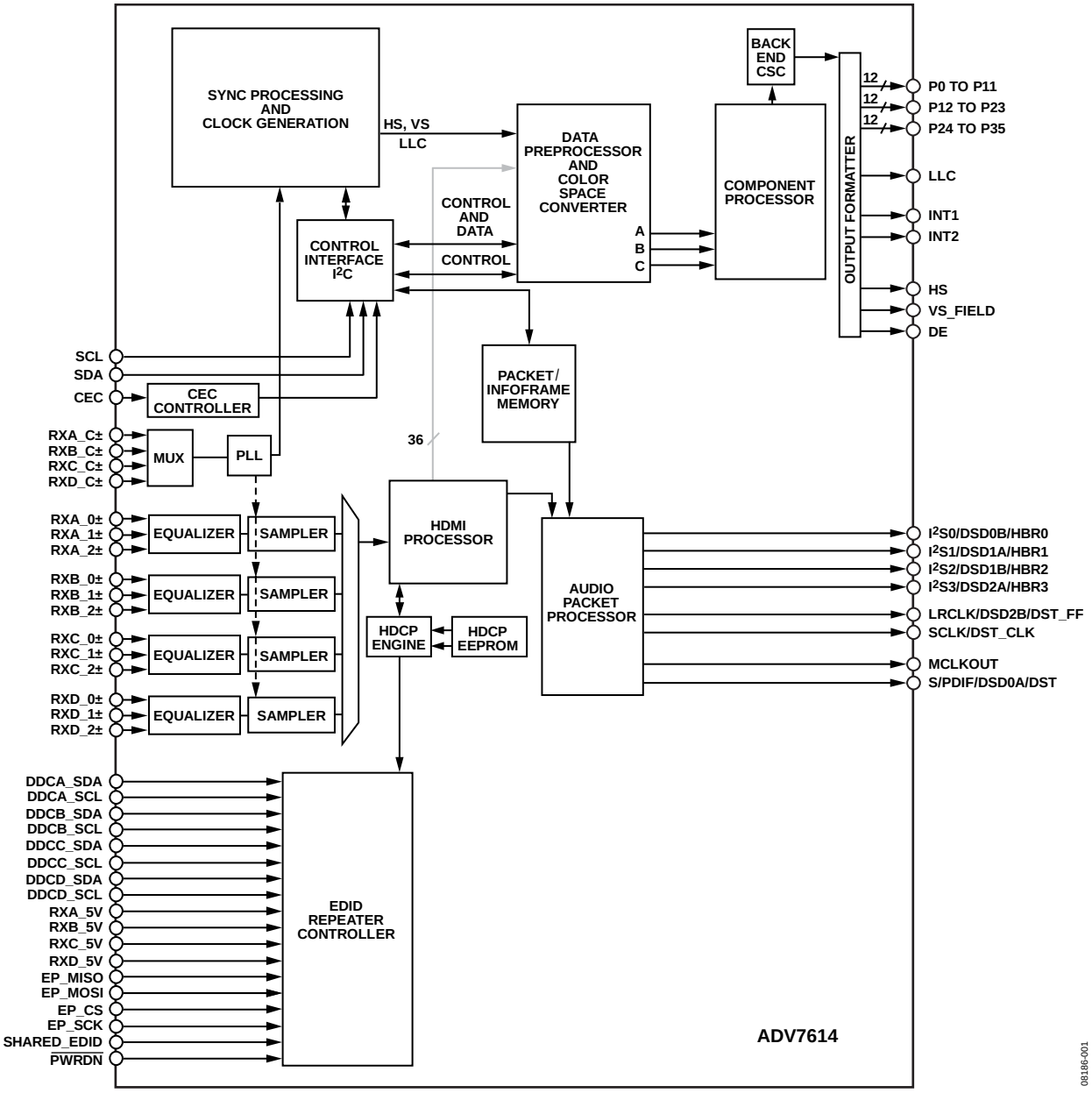


Figure 1.

SPECIFICATIONS

DVDD = 1.8 V ± 5%, DVDDIO = 3.3 V ± 5%, PVDD = 1.8 V ± 5%, TVDD = 3.3 V ± 5%, CVDD = 1.8 V ± 5%, T_{MIN} to T_{MAX} = −40°C to +70°C, unless otherwise noted.

ANALOG, DIGITAL, HDMI, AND AC SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUTS					
Input High Voltage (V_{IH})		2			V
Input Low Voltage (V_{IL})				0.8	V
Input Current (I_{IN})	$\overline{\text{RESET}}$ pin	−60		+60	µA
	Other digital inputs	−10		+10	µA
Input Capacitance (C_{IN})				10	pF
DIGITAL INPUTS (5 V TOLERANT)[1]					
Input High Voltage (V_{IH})		2.6			V
Input Low Voltage (V_{IL})				0.8	V
Input Current (I_{IN})	SHARED_EDID pin	−150		+60	µA
	Other 5 V digital inputs	−82		+82	µA
DIGITAL OUTPUTS					
Output High Voltage (V_{OH})		2.4			V
Output Low Voltage (V_{OL})				0.4	V
High Impedance Leakage Current (I_{LEAK})			10		µA
Output Capacitance (C_{OUT})				20	pF
HDMI					
TMDS Differential Pin Capacitance			0.3		pF
AC SPECIFICATIONS					
Intrapair (+ to −) Differential Input Skew for TMDS Clock Rates up to 222.75 MHz		0.4 T_{BIT}			ps
Intrapair (+ to −) Differential Input Skew for TMDS Clock Rates Above 222.75 MHz		0.15 T_{BIT} + 112			ps
Channel-to-Channel Differential Input Skew				0.2 t_{PIXEL} + 1.78	ns
TMDS Input Clock Range		25		225	MHz
Input Clock Jitter Tolerance			0.5	0.25 T_{BIT}	T_{BIT}

[1] The following pins are 5 V tolerant: DDCA_SCL, DDCA_SDA, DDCB_SCL, DDCB_SDA, DDCC_SCL, DDCC_SDA, DDCD_SCL, DDCD_SDA, RXA_5V, RXB_5V, RXC_5V, RXD_5V, SHARED_EDID, $\overline{\text{PWRDN}}$, EP_MISO.

DATA AND I²C TIMING CHARACTERISTICS

DVDD = 1.8 V ± 5%, DVDDIO = 3.3 V ± 5%, PVDD = 1.8 V ± 5%, TVDD = 3.3 V ± 5%, CVDD = 1.8 V ± 5%, T_{MIN} to T_{MAX} = −40°C to +70°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
VIDEO SYSTEM CLOCK AND CRYSTAL						
Crystal Nominal Frequency				24.576/28.6363		MHz
Crystal Frequency Stability					±50	ppm
LLC Frequency Range			12.825		170	MHz
External Clock Source [1]		External crystal must operate at 1.8 V				
Input High Voltage	V_{IH}	Ball H15 (XTALP) driven with external clock source	1.2			V
Input Low Voltage	V_{IL}	Ball H15 (XTALP) driven with external clock source			0.4	V
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
I²C PORTS (FAST MODE)						
xCL Frequency [2]					400	kHz
xCL Minimum Pulse Width High [2]	t_1		600			ns
xCL Minimum Pulse Width Low [2]	t_2		1.3			µs
Hold Time (Start Condition)	t_3		600			ns
Setup Time (Start Condition)	t_4		600			ns
xDA Setup Time [2]	t_5		100			ns
xCL and xDA Rise Time [2]	t_6				300	ns
xCL and xDA Fall Time [2]	t_7				300	ns
Setup Time (Stop Condition)	t_8		0.6			µs
I²C PORTS (NORMAL MODE)						
xCL Frequency [2]					100	kHz
xCL Minimum Pulse Width High [2]	t_1		4.0			µs
xCL Minimum Pulse Width Low [2]	t_2		4.7			µs
Hold Time (Start Condition)	t_3		4.0			µs
Setup Time (Start Condition)	t_4		4.7			µs
xDA Setup Time [2]	t_5		250			ns
xCL and xDA Rise Time [2]	t_6				1000	ns
xCL and xDA Fall Time [2]	t_7				300	ns
Setup Time (Stop Condition)	t_8		4.0			µs
DATA AND CONTROL OUTPUTS [3]						
Data Output Transition Time SDR (CP)	t_{11}	End of valid data to negative clock edge		0.55		ns
Data Output Transition Time SDR (CP)	t_{12}	Negative clock edge to start of valid data		1.0		ns
VIDEO I²S PORT						
Master Mode						
SCLK Mark Space Ratio	t_{13}:t_{14}		45:55		55:45	% duty cycle
LRCLK Data Transition Time	t_{15}	End of valid data to negative SCLK edge			10	ns
LRCLK Data Transition Time	t_{16}	Negative SCLK edge to start of valid data			10	ns
I2Sx Data Transition Time [4]	t_{17}	End of valid data to negative SCLK edge			5	ns
I2Sx Data Transition Time [4]	t_{18}	Negative SCLK edge to start of valid data			5	ns

[1] The XTAL_CTRL bit must be enabled for external oscillator operation. A 1.8 V oscillator must be used.
[2] The prefix x refers to S, DDCA_S, DDCB_S, DDCC_S, and DDCD_S.
[3] LLC DLL disabled.
[4] The suffix x refers to 0, 1, 2, and 3.

POWER SPECIFICATIONS

DVDD = 1.8 V ± 5%, DVDDIO = 3.3 V ± 5%, PVDD = 1.8 V ± 5%, TVDD = 3.3 V ± 5%, CVDD = 1.8 V ± 5%, T_{MIN} to T_{MAX} = −40°C to +70°C, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLIES					
Digital Core Power Supply (DVDD)	1.71	1.8	1.89	V	
Digital I/O Power Supply (DVDDIO)	3.14	3.3	3.46	V	
PLL Power Supply (PVDD)	1.71	1.8	1.89	V	
Terminator Power Supply (TVDD)	3.14	3.3	3.46	V	
Comparator Power Supply (CVDD)	1.71	1.8	1.89	V	
CURRENT CONSUMPTION[1, 2, 3, 4]					
Comparator Power Supply (I_{CVDD})		102.9	121.9	mA	1080p 12-bit Deep Color with 4-channel PCM
		3.7	4.0	mA	Power-Down Mode 0
Digital Core Power Supply (I_{DVDD})		212.4	290.2	mA	1080p 12-bit Deep Color with 4-channel PCM
		2.3	2.5	mA	Power-Down Mode 0
Digital I/O Power Supply (I_{DVDDIO})		29.7	167.0	mA	1080p 12-bit Deep Color with 4-channel PCM
		1.3	1.4	mA	Power-Down Mode 0
PLL Power Supply (I_{PVDD})		74.7	87.5	mA	1080p 12-bit Deep Color with 4-channel PCM
		0.2	0.22	mA	Power-Down Mode 0
Termination Power Supply (I_{TVDD})		185.3	204.5	mA	1080p 12-bit Deep Color with 4-channel PCM
		1.1	1.2	mA	Power-Down Mode 0

[1] All maximum current values are guaranteed by characterization to assist in power supply design.
[2] Typical current consumption values are recorded with nominal voltage supply levels and a SMPTEBAR pattern.
[3] Maximum current consumption values are recorded with maximum rated voltage supply levels and a Moire X pattern.
[4] Termination power supply includes TVDD current consumed off chip.

Timing Diagrams

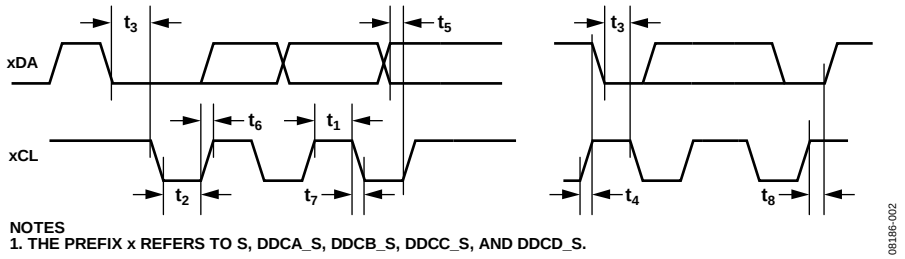


Figure 2. I^2C Timing

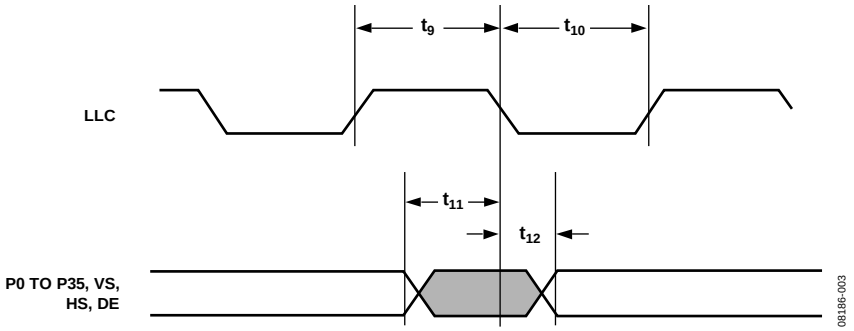
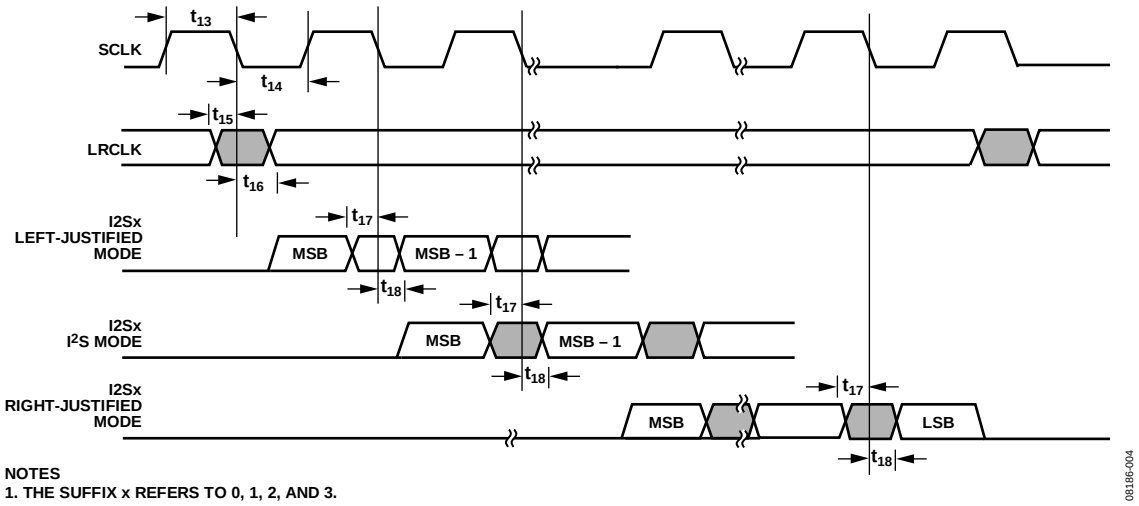


Figure 3. Pixel Port and Control SDR Output Timing



NOTES
1. THE SUFFIX x REFERS TO 0, 1, 2, AND 3.

Figure 4. I²S Timing

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
DVDD to GND	2.2 V
PVDD to GND	2.2 V
DVDDIO to GND	4.0 V
CVDD to GND	2.2 V
TVDD to GND	4.0 V
Digital Inputs Voltage to GND	GND – 0.3 V to DVDDIO + 0.3 V
5 V Tolerant Digital Inputs to GND[1]	5.3 V
Digital Output Voltage to GND	GND – 0.3 V to DVDDIO + 0.3 V
XTAL Pins	–0.3 V to PVDD to 0.3 V
Maximum Junction Temperature ($T_{J\ MAX}$)	125°C
Storage Temperature	150°C
Infrared Reflow Soldering (20 sec)	260°C

[1] The following inputs are 3.3 V inputs but are 5 V tolerant: DDCA_SCL, DDCA_SDA, DDCB_SCL, DDCB_SDA, DDCC_SCL, DDCC_SDA, DDCD_SCL, DDCD_SDA, RXA_5V, RXB_5V, RXC_5V, RXD_5V, SHARED_EDID, PWRDN, EP_MISO.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the ADV7614, the user is advised to turn off unused sections of the part.

Due to printed circuit board (PCB) metal variation and, thus, variation in PCB heat conductivity, the value of θ_{JA} may differ for various PCBs.

The most efficient measurement solution is obtained using the package surface temperature to estimate the die temperature because this eliminates the variance associated with the θ_{JA} value.

The maximum junction temperature ($T_{J\ MAX}$) of 125°C must not be exceeded. The following equation calculates the junction temperature using the measured package surface temperature and applies only when no heat sink is used on the device under test (DUT):

$$T_J = T_S + (\Psi_{JT} \times W_{TOTAL})$$

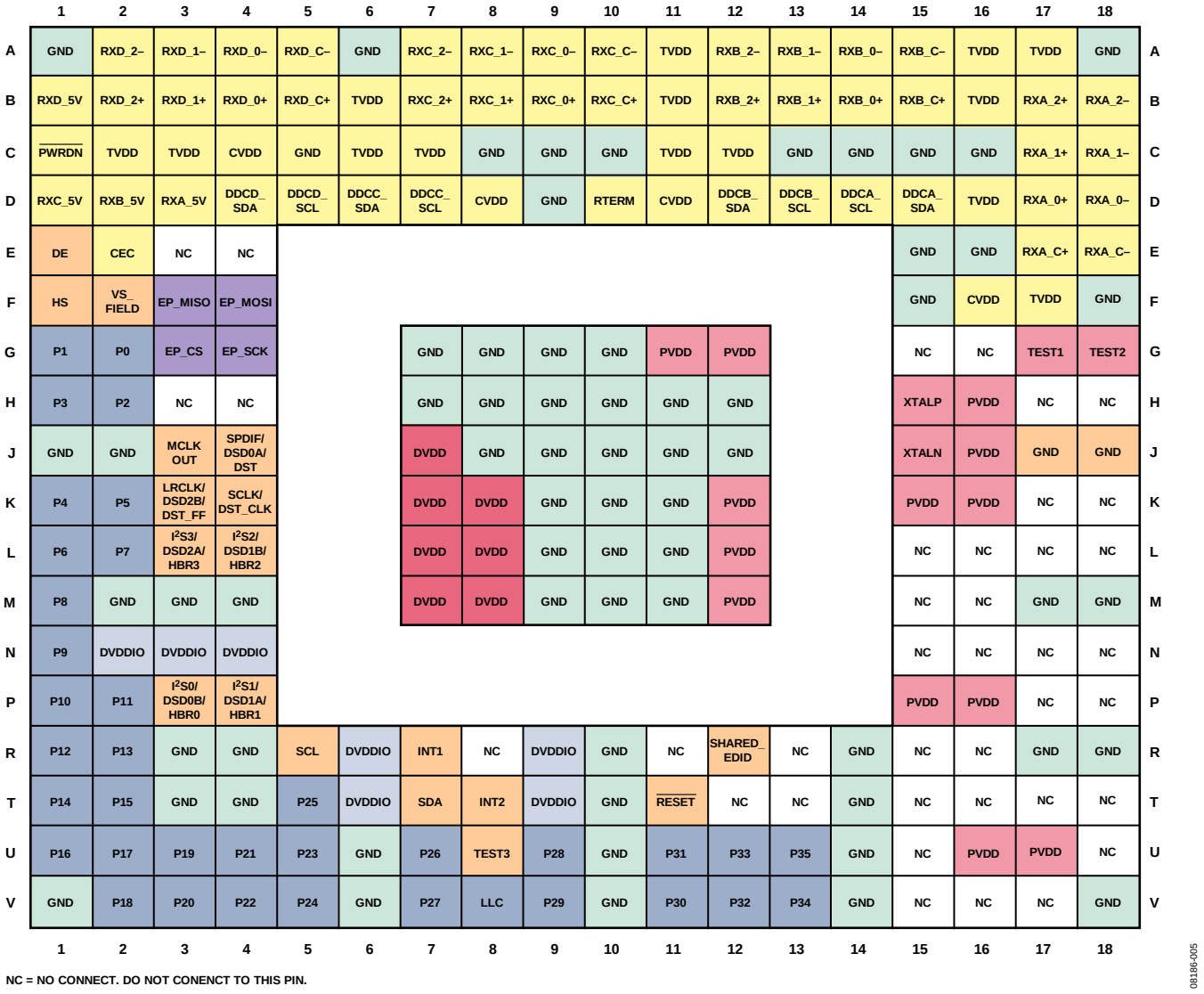
where:
T_S is the package surface temperature (°C).
Ψ_{JT} = 0.3°C/W for a 260-ball CSP_BGA.
$W_{TOTAL} = ((PVDD \times I_{PVDD}) + (0.05 \times TVDD \times I_{TVDD}) + (CVDD \times I_{CVDD}) + (DVDD \times I_{DVDD}) + (DVDDIO \times I_{DVDDIO}))$.

Note that for W_{TOTAL}, 5% of TVDD power is dissipated on the part itself.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NC = NO CONNECT. DO NOT CONENCT TO THIS PIN.

Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	GND	Ground	Ground.
A2	RXD_2–	HDMI input	Digital Input Channel 2 Complement of Port D in the HDMI Interface.
A3	RXD_1–	HDMI input	Digital Input Channel 1 Complement of Port D in the HDMI Interface.
A4	RXD_0–	HDMI input	Digital Input Channel 0 Complement of Port D in the HDMI Interface.
A5	RXD_C–	HDMI input	Digital Input Clock Complement of Port D in the HDMI Interface.
A6	GND	Ground	Ground.
A7	RXC_2–	HDMI input	Digital Input Channel 2 Complement of Port C in the HDMI Interface.
A8	RXC_1–	HDMI input	Digital Input Channel 1 Complement of Port C in the HDMI Interface.
A9	RXC_0–	HDMI input	Digital Input Channel 0 Complement of Port C in the HDMI Interface.
A10	RXC_C–	HDMI input	Digital Input Clock Complement of Port C in the HDMI Interface.
A11	TVDD	Power	Terminator Supply Voltage (3.3 V).
A12	RXB_2–	HDMI input	Digital Input Channel 2 Complement of Port B in the HDMI Interface.

Pin No.	Mnemonic	Type	Description
A13	RXB_1−	HDMI input	Digital Input Channel 1 Complement of Port B in the HDMI Interface.
A14	RXB_0−	HDMI input	Digital Input Channel 0 Complement of Port B in the HDMI Interface.
A15	RXB_C−	HDMI input	Digital Input Clock Complement of Port B in the HDMI Interface.
A16	TVDD	Power	Terminator Supply Voltage (3.3 V).
A17	TVDD	Power	Terminator Supply Voltage (3.3 V).
A18	GND	Ground	Ground.
B1	RXD_5V	HDMI input	5 V Detect Pin for Port D in the HDMI Interface.
B2	RXD_2+	HDMI input	Digital Input Channel 2 True of Port D in the HDMI Interface.
B3	RXD_1+	HDMI input	Digital Input Channel 1 True of Port D in the HDMI Interface.
B4	RXD_0+	HDMI input	Digital Input Channel 0 True of Port D in the HDMI Interface.
B5	RXD_C+	HDMI input	Digital Input Clock True of Port D in the HDMI Interface.
B6	TVDD	Power	Terminator Supply Voltage (3.3 V).
B7	RXC_2+	HDMI input	Digital Input Channel 2 True of Port C in the HDMI Interface.
B8	RXC_1+	HDMI input	Digital Input Channel 1 True of Port C in the HDMI Interface.
B9	RXC_0+	HDMI input	Digital Input Channel 0 True of Port C in the HDMI Interface.
B10	RXC_C+	HDMI input	Digital Input Clock True of Port C in the HDMI Interface.
B11	TVDD	Power	Terminator Supply Voltage (3.3 V).
B12	RXB_2+	HDMI input	Digital Input Channel 2 True of Port B in the HDMI Interface.
B13	RXB_1+	HDMI input	Digital Input Channel 1 True of Port B in the HDMI Interface.
B14	RXB_0+	HDMI input	Digital Input Channel 0 True of Port B in the HDMI Interface.
B15	RXB_C+	HDMI input	Digital Input Clock True of Port B in the HDMI Interface.
B16	TVDD	Power	Terminator Supply Voltage (3.3 V).
B17	RXA_2+	HDMI input	Digital Input Channel 2 True of Port A in the HDMI Interface.
B18	RXA_2−	HDMI input	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
C1	$\overline{\text{PWRDN}}$	Digital input	Active Low System Power Detect. If low, EDID can be powered from a 5 V signal of the HDMI port when connected to active equipment.
C2	TVDD	Power	Terminator Supply Voltage (3.3 V).
C3	TVDD	Power	Terminator Supply Voltage (3.3 V).
C4	CVDD	Power	Comparator Supply Voltage (1.8 V).
C5	GND	Ground	Ground.
C6	TVDD	Power	Terminator Supply Voltage (3.3 V).
C7	TVDD	Power	Terminator Supply Voltage (3.3 V).
C8	GND	Ground	Ground.
C9	GND	Ground	Ground.
C10	GND	Ground	Ground.
C11	TVDD	Power	Terminator Supply Voltage (3.3 V).
C12	TVDD	Power	Terminator Supply Voltage (3.3 V).
C13	GND	Ground	Ground.
C14	GND	Ground	Ground.
C15	GND	Ground	Ground.
C16	GND	Ground	Ground.
C17	RXA_1+	HDMI input	Digital Input Channel 1 True of Port A in the HDMI interface.
C18	RXA_1−	HDMI input	Digital Input Channel 1 Complement of Port A in the HDMI interface.
D1	RXC_5V	HDMI input	5 V Detect Pin for Port C in the HDMI Interface.
D2	RXB_5V	HDMI input	5 V Detect Pin for Port B in the HDMI Interface.
D3	RXA_5V	HDMI input	5 V Detect Pin for Port A in the HDMI Interface.
D4	DDCD_SDA	HDMI input	HDCP Slave Serial Data Port D. DDCD_SDA is a 3.3 V input that is 5 V tolerant.
D5	DDCD_SCL	HDMI input	HDCP Slave Serial Clock Port D. DDCD_SCL is a 3.3 V input that is 5 V tolerant.
D6	DDCC_SDA	HDMI input	HDCP Slave Serial Data Port C. DDCC_SDA is a 3.3 V input that is 5 V tolerant.
D7	DDCC_SCL	HDMI input	HDCP Slave Serial Clock Port C. DDCC_SCL is a 3.3 V input that is 5 V tolerant.
D8	CVDD	Power	Comparator Supply Voltage (1.8 V).
D9	GND	Ground	Ground.
D10	RTERM	Miscellaneous analog	This pin sets internal termination resistance. Use a 500 Ω resistor between this pin and GND.

Pin No.	Mnemonic	Type	Description
D11	CVDD	Power	Comparator Supply Voltage (1.8 V).
D12	DDCB_SDA	HDMI input	HDCP Slave Serial Data Port B. DDCB_SDA is a 3.3 V input that is 5 V tolerant.
D13	DDCB_SCL	HDMI input	HDCP Slave Serial Clock Port B. DDCB_SCL is a 3.3 V input that is 5 V tolerant.
D14	DDCA_SCL	HDMI input	HDCP Slave Serial Clock Port A. DDCA_SCL is a 3.3 V input that is 5 V tolerant.
D15	DDCA_SDA	HDMI input	HDCP Slave Serial Data Port A. DDCA_SDA is a 3.3 V input that is 5 V tolerant.
D16	TVDD	Power	Terminator Supply Voltage (3.3 V).
D17	RXA_0+	HDMI input	Digital Input Channel 0 True of Port A in the HDMI Interface.
D18	RXA_0−	HDMI input	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
E1	DE	Digital video output	Data Enable. DE is a signal that indicates active pixel data.
E2	CEC	Digital I/O	Consumer Electronic Control Channel.
E3	NC	No connect	Do Not Connect.
E4	NC	No connect	Do Not Connect.
E15	GND	Ground	Ground.
E16	GND	Ground	Ground.
E17	RXA_C+	HDMI input	Digital Input Clock True of Port A in the HDMI Interface.
E18	RXA_C−	HDMI input	Digital Input Clock Complement of Port A in the HDMI Interface.
F1	HS	Digital video output	Horizontal Synchronization Output Signal in the HDMI Processor.
F2	VS_FIELD	Digital video output	VS is a vertical synchronization output signal in the HDMI processor. FIELD is a field synchronization output signal in all interlaced video modes. VS or FIELD can be configured for this pin.
F3	EP_MISO	Digital input	SPI Master Input/Slave Output for External EDID Interface.
F4	EP_MOSI	Digital output	SPI Master Output/Slave Input for External EDID Interface.
F15	GND	Ground	Ground.
F16	CVDD	Power	Comparator Supply Voltage (1.8 V).
F17	TVDD	Power	Terminator Supply Voltage (3.3 V).
F18	GND	Ground	Ground.
G1	P1	Digital video output	Video Pixel Output Port.
G2	P0	Digital video output	Video Pixel Output Port.
G3	EP_CS	Digital output	SPI Chip Select for External EDID Interface.
G4	EP_SCK	Digital output	SPI Clock for External EDID Interface.
G7	GND	Ground	Ground.
G8	GND	Ground	Ground.
G9	GND	Ground	Ground.
G10	GND	Ground	Ground.
G11	PVDD	Power	PLL Supply Voltage (1.8 V).
G12	PVDD	Power	PLL Supply Voltage (1.8 V).
G15	NC	No connect	Do Not Connect.
G16	NC	No connect	Do Not Connect.
G17	TEST1	Test	Connect to GND through a 10 kΩ resistor.
G18	TEST2	Test	Connect to GND through a 10 kΩ resistor.
H1	P3	Digital video output	Video Pixel Output Port.
H2	P2	Digital video output	Video Pixel Output Port.
H3	NC	No connect	Do Not Connect.
H4	NC	No connect	Do Not Connect.
H7	GND	Ground	Ground.
H8	GND	Ground	Ground.
H9	GND	Ground	Ground.
H10	GND	Ground	Ground.
H11	GND	Ground	Ground.
H12	GND	Ground	Ground.
H15	XTALP	Miscellaneous analog	This is the input pin for the 28.6363 MHz crystal, or it can be overdriven by an external 1.8 V, 28.6363 MHz clock oscillator source to clock the ADV7614. A crystal frequency of 24.576 MHz is also supported.
H16	PVDD	Power	PLL Supply Voltage (1.8 V).

Pin No.	Mnemonic	Type	Description
H17	NC	No connect	Do Not Connect.
H18	NC	No connect	Do Not Connect.
J1	GND	Ground	Ground.
J2	GND	Ground	Ground.
J3	MCLKOUT	Digital output	Audio Master Clock Output.
J4	S/PDIF/DSD0A/DST	Digital output	S/PDIF Digital Audio Output (S/PDIF). First DSD Data Channel (DSD0A). DST Stream (DST).
J7	DVDD	Power	Digital Supply Voltage (1.8 V).
J8	GND	Ground	Ground.
J9	GND	Ground	Ground.
J10	GND	Ground	Ground.
J11	GND	Ground	Ground.
J12	GND	Ground	Ground.
J15	XTALN	Miscellaneous analog	This pin should be connected to the 28.6363 MHz crystal or left as a no connect pin if an external 1.8 V, 28.6363 MHz clock oscillator source is used to clock the ADV7614. In crystal mode, the crystal must be a fundamental crystal. A crystal frequency of 24.576 MHz is also supported.
J16	PVDD	Power	PLL Supply Voltage (1.8 V).
J17	GND	Ground	Ground.
J18	GND	Ground	Ground.
K1	P4	Digital video output	Video Pixel Output Port.
K2	P5	Digital video output	Video Pixel Output Port.
K3	LRCLK/DSD2B/DST_FF	Digital output	Data Output Clock. Left and Right Audio Channels (LRCLK). Sixth DSD Data Channel (DSD2B). DST Frame (DST_FF).
K4	SCLK/DST_CLK	Digital output	Audio Serial Clock Output (SCLK). DST Clock (DST_CLK).
K7	DVDD	Power	Digital Supply Voltage (1.8 V).
K8	DVDD	Power	Digital Supply Voltage (1.8 V).
K9	GND	Ground	Ground.
K10	GND	Ground	Ground.
K11	GND	Ground	Ground.
K12	PVDD	Power	PLL Supply Voltage (1.8 V).
K15	PVDD	Power	PLL Supply Voltage (1.8 V).
K16	PVDD	Power	PLL Supply Voltage (1.8 V).
K17	NC	No connect	Do Not Connect.
K18	NC	No connect	Do Not Connect.
L1	P6	Digital video output	Video Pixel Output Port.
L2	P7	Digital video output	Video Pixel Output Port.
L3	I^2S3/DSD2A/HBR3	Digital output	I^2S Audio (Channel 7 and Channel 8) (I^2S3). Fifth DSD Data Channel (DSD2A). Fourth Block of HBR Stream (HBR3).
L4	I^2S2/DSD1B/HBR2	Digital output	I^2S Audio (Channel 5 and Channel 6) (I^2S2). Fourth DSD Data Channel (DSD1B). Third Block of HBR Stream (HBR2).
L7	DVDD	Power	Digital Supply Voltage (1.8 V).
L8	DVDD	Power	Digital Supply Voltage (1.8 V).
L9	GND	Ground	Ground.
L10	GND	Ground	Ground.
L11	GND	Ground	Ground.
L12	PVDD	Power	PLL Supply Voltage (1.8 V).
L15	NC	No connect	Do Not Connect.
L16	NC	No connect	Do Not Connect.

Pin No.	Mnemonic	Type	Description
L17	NC	No connect	Do Not Connect.
L18	NC	No connect	Do Not Connect.
M1	P8	Digital video output	Video Pixel Output Port.
M2	GND	Ground	Ground.
M3	GND	Ground	Ground.
M4	GND	Ground	Ground.
M7	DVDD	Power	Digital Supply Voltage (1.8 V).
M8	DVDD	Power	Digital Supply Voltage (1.8 V).
M9	GND	Ground	Ground.
M10	GND	Ground	Ground.
M11	GND	Ground	Ground.
M12	PVDD	Power	PLL Supply Voltage (1.8 V).
M15	NC	No connect	Do Not Connect.
M16	NC	No connect	Do Not Connect.
M17	GND	Ground	Ground.
M18	GND	Ground	Ground.
N1	P9	Digital video output	Video Pixel Output Port.
N2	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
N3	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
N4	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
N15	NC	No connect	Do Not Connect.
N16	NC	No connect	Do Not Connect.
N17	NC	No connect	Do Not Connect.
N18	NC	No connect	Do Not Connect.
P1	P10	Digital video output	Video Pixel Output Port.
P2	P11	Digital video output	Video Pixel Output Port.
P3	I^2S0/DSD0B/HBR0	Digital output	I^2S Audio (Channel 1 and Channel 2) (I^2S0). Second DSD Data Channel (DSD0B). First Block of HBR Stream (HBR0).
P4	I^2S1/DSD1A/HBR1	Digital output	I^2S Audio (Channel 3 and Channel 4) (I^2S1). Third DSD Data Channel (DSD1A). Second Block of HBR Stream (HBR1).
P15	PVDD	Power	PLL Supply Voltage (1.8 V).
P16	PVDD	Power	PLL Supply Voltage (1.8 V).
P17	NC	No connect	Do Not Connect.
P18	NC	No connect	Do Not Connect.
R1	P12	Digital video output	Video Pixel Output Port.
R2	P13	Digital video output	Video Pixel Output Port.
R3	GND	Ground	Ground.
R4	GND	Ground	Ground.
R5	SCL	Digital I/O	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz. SCL is the clock line for the control port.
R6	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
R7	INT1	Digital output	Interrupt Pin 1. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user control.
R8	NC	No connect	Do Not Connect.
R9	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
R10	GND	Ground	Ground.
R11	NC	No connect	Do Not Connect.
R12	SHARED_EDID	Digital input	EDID Flag. When high, all four HDMI ports share a common EDID. When low, Port D does not share a common EDID; Port D operates with a separate EDID.
R13	NC	No connect	Do Not Connect.
R14	GND	Ground	Ground.
R15	NC	No connect	Do Not Connect.

Pin No.	Mnemonic	Type	Description
R16	NC	No connect	Do Not Connect.
R17	GND	Ground	Ground.
R18	GND	Ground	Ground.
T1	P14	Digital video output	Video Pixel Output Port.
T2	P15	Digital video output	Video Pixel Output Port.
T3	GND	Ground	Ground.
T4	GND	Ground	Ground.
T5	P25	Digital video output	Video Pixel Output Port.
T6	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
T7	SDA	Digital I/O	I^2C Port Serial Data Input/Output Pin. SDA is the data line for the control port.
T8	INT2	Digital output	Interrupt Pin 2. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user control.
T9	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
T10	GND	Ground	Ground.
T11	$\overline{\text{RESET}}$	Digital input	Chip Reset. Active low. The minimum low time for a reset to take place is 5 ms.
T12	NC	No connect	Do Not Connect.
T13	NC	No connect	Do Not Connect.
T14	GND	Ground	Ground.
T15	NC	No connect	Do Not Connect.
T16	NC	No connect	Do Not Connect.
T17	NC	No connect	Do Not Connect.
T18	NC	No connect	Do Not Connect.
U1	P16	Digital video output	Video Pixel Output Port.
U2	P17	Digital video output	Video Pixel Output Port.
U3	P19	Digital video output	Video Pixel Output Port.
U4	P21	Digital video output	Video Pixel Output Port.
U5	P23	Digital video output	Video Pixel Output Port.
U6	GND	Ground	Ground.
U7	P26	Digital video output	Video Pixel Output Port.
U8	TEST3	Test	Connect to GND through a 10 kΩ resistor.
U9	P28	Digital video output	Video Pixel Output Port.
U10	GND	Ground	Ground.
U11	P31	Digital video output	Video Pixel Output Port.
U12	P33	Digital video output	Video Pixel Output Port.
U13	P35	Digital video output	Video Pixel Output Port.
U14	GND	Ground	Ground.
U15	NC	No connect	Do Not Connect.
U16	PVDD	Power	PLL Supply Voltage (1.8 V).
U17	PVDD	Power	PLL Supply Voltage (1.8 V).
U18	NC	No connect	Do Not Connect.
V1	GND	Ground	Ground.
V2	P18	Digital video output	Video Pixel Output Port.
V3	P20	Digital video output	Video Pixel Output Port.
V4	P22	Digital video output	Video Pixel Output Port.
V5	P24	Digital video output	Video Pixel Output Port.
V6	GND	Ground	Ground.
V7	P27	Digital video output	Video Pixel Output Port.
V8	LLC	Digital video output	Line-Locked Output Clock for the Pixel Data (Range Is 13.5 MHz to 170 MHz).
V9	P29	Digital video output	Video Pixel Output Port.
V10	GND	Ground	Ground.
V11	P30	Digital video output	Video Pixel Output Port.
V12	P32	Digital video output	Video Pixel Output Port.
V13	P34	Digital video output	Video Pixel Output Port.

Pin No.	Mnemonic	Type	Description
V14	GND	Ground	Ground.
V15	NC	No connect	Do Not Connect.
V16	NC	No connect	Do Not Connect.
V17	NC	No connect	Do Not Connect.
V18	GND	Ground	Ground.

FUNCTIONAL OVERVIEW

HDMI RECEIVER

The HDMI receiver on the ADV7614 incorporates active equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies. The equalization is programmable. It is capable of equalizing for cable lengths up to 30 meters to achieve robust receiver performance at even the highest HDMI data rates. The HDMI receiver supports all HDTV formats up to 1080p and all display resolutions up to UXGA (1600 × 1200 at 60 Hz).

With the inclusion of HDCP, displays can receive encrypted video content. The HDMI interface of the ADV7614 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission as specified by the HDCP 1.3 protocol.

The HDMI receiver offers advanced audio functionality. It supports multichannel I²S audio for up to eight channels. It also supports a six-DSD channel interface with each channel carrying an oversampled 1-bit representation of the audio signal as delivered on SACD. It incorporates a DST interface that outputs audio data decoded from DST audio packets. The ADV7614 can also receive HBR audio packet streams and outputs them through the HBR interface in an S/PDIF format conforming to the IEC60958 standard. It supports multichannel I²S audio for up to eight channels. The receiver also contains an audio mute controller that can detect a variety of conditions that may result in audible extraneous noise in the audio output. On detection of these conditions, the audio data can be ramped to prevent audio clicks or pops.

COMPONENT PROCESSOR (CP)

The video standards supported by the CP are 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, 1250i, VGA up to UXGA at 60 Hz, and many other standards.

Automatic adjustments within the CP include gain (contrast) and offset (brightness); manual adjustment controls are also supported.

A fully programmable any-to-any 3 × 3 color space conversion (CSC) matrix is placed between the HDMI processor and the CP section. This enables YCrCb-to-RGB and YCrCb-to-RGB conversions. Many other standards of color space can be implemented using the color space converter.

CP PIXEL DATA OUTPUT MODES

The output section of the CP is highly flexible. It can be configured in an SDR mode with one data packet per clock cycle or in a DDR mode where data is presented on the rising and falling edge of the clock. In SDR mode, a 16-/20-/24-bit 4:2:2 or 24-/30-/36-bit 4:4:4 output is possible. In these modes, the HS, VS, FIELD, and DE (where applicable) timing reference signals are provided. In DDR mode, the ADV7614 can be configured in an 8-/10-/12-bit 4:2:2 YCrCb or 12-bit 4:4:4 RGB/YCrCb pixel output interface with corresponding timing signals.

I²C INTERFACE

The ADV7614 supports a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. The ADV7614 is controlled by an external I²C master device, such as a microcontroller.

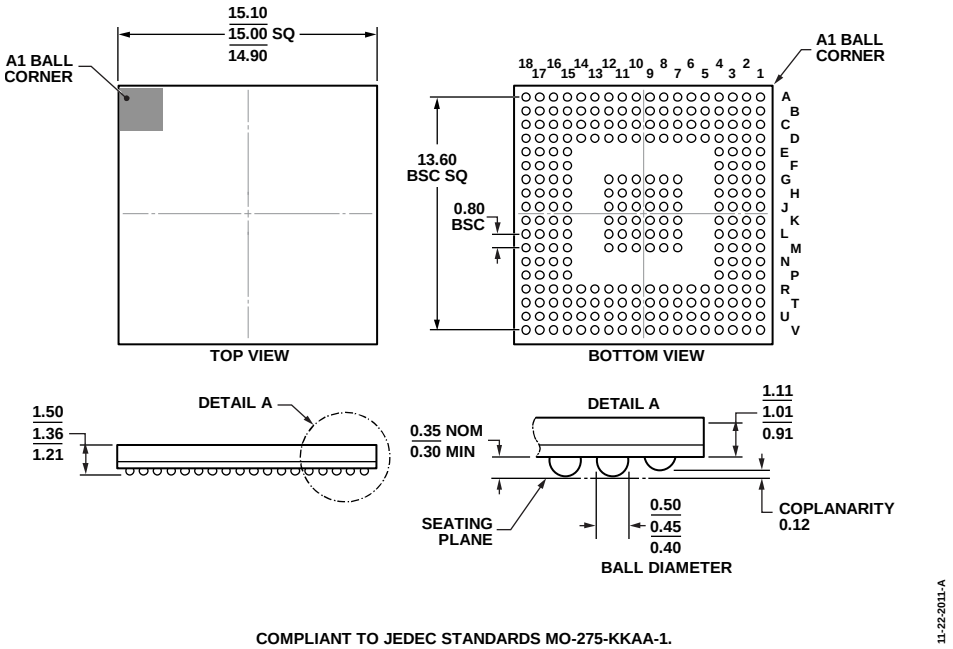
OTHER FEATURES

In addition to HS, VS, and FIELD output signals with programmable position, polarity, and width, the ADV7614 provides the following:

- Programmable interrupt request output pins: INT1 and INT2
- Low power consumption: 1.8 V digital core, 3.3 V digital input/output, low power power-down mode, and green PC mode
- 15 mm × 15 mm, RoHS-compliant BGA package

For more detailed product information about the ADV7614, contact a local Analog Devices, Inc., sales office.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-KKAA-1.

Figure 6. 260-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-260-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADV7614BBCZ	−40°C to +70°C	260-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-260-1
EVAL-ADV7614EB1Z		ADV7614BBCZ Front-End Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The ADV7614BBCZ is programmed with internal HDCP keys. Customers must have HDCP adopter status (consult Digital Content Protection, LLC, for licensing requirements) to purchase any components with internal HDCP keys.

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I²C refers to a communications protocol originally developed by Phillips Semiconductors (now NXP Semiconductors).

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