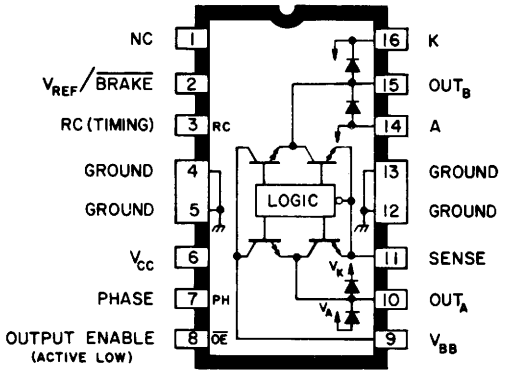
2953 AND 2954

Data Sheet 29319.2B

FULL-BRIDGE PWM MOTOR DRIVERS

UDN2953B



Dwg. No. A-13,024

ABSOLUTE MAXIMUM RATINGS at T_J = +150°C

Motor Supply Voltage, V_{BB} . . . . . 50 V
Output Current, I_{OUT}
(Peak) . . . . . ±3.5 A
(Continuous) . . . . . ±2.0 A
Load Diode Voltage, V_K . . . . . V_{BB}
Minimum Clamp Diode Voltage,
V_A . . . . . Ground
Logic Supply Voltage, V_{CC} . . . . . 7.0 V
Logic Input Voltage,
V_{PHASE}, V_{ENABLE} . . . . . V_{BB}
Sense Voltage, V_{SENSE} . . . . . 1.5 V
Reference Voltage, V_{REF}/BRAKE . . . . . 15 V
Package Power Dissipation,
P_D . . . . . See Graphs
Operating Temperature Range,
T_A . . . . . -20°C to +85°C
Storage Temperature Range,
T_S . . . . . -55°C to +150°C

The UDN2953B and UDN2954W are designed for bidirectional control of dc or stepper motors with continuous output currents to 2 A and peak start-up currents as high as 3.5 A. For pulse-width modulated (chopped-mode) operation, the output current is determined by the user's selection of a reference voltage and sensing resistor while the OFF pulse duration is set by an external RC timing network. PWM operation is characterized by maximum efficiency and low power-dissipation levels. Extensive internal circuit protection includes thermal shutdown with hysteresis, transient-suppression diodes, and crossover current protection.

When the V_{REF}/BRAKE pin is low (<0.6 V), the braking function is enabled. This turns both sink drivers OFF and the source drivers are turned ON. When V_{REF}/BRAKE is set above 2.4 V, that voltage (and the current sensing resistor) determines the load current trip point. An RC TIMING pin is available to use for an internal one-shot to control load current decay time.

The UDN2953B driver is supplied in a 16-pin dual-in-line plastic package with copper heat-sink contact tabs. The lead configuration enables easy attachment of a heat sink while fitting a standard integrated circuit socket or printed wiring board layout. The UDN2954W, for high-power package power dissipation requirements, is supplied in a 12-pin single in-line power tab package. In any package style, the heat sink is at ground potential and needs no insulation.

FEATURES

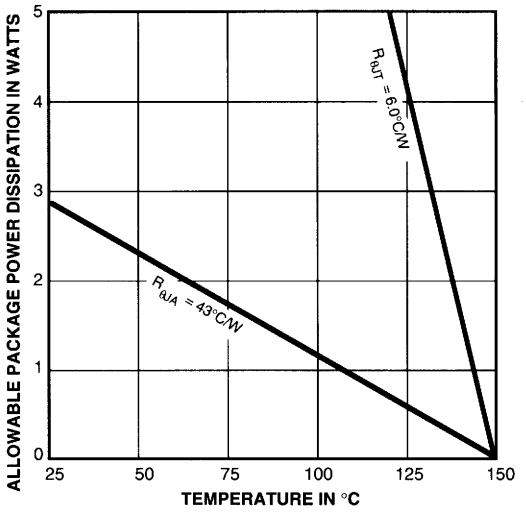
- 50 V Output Voltage Rating
- 2 A Continuous Output Rating
- Internal Flyback Diodes
- Thermal Shutdown
- Crossover Current Protection
- BRAKE, ENABLE, and Current-Limit Functions

Always order by complete part number:

Part Number	Package
UDN2953B	16-Pin DIP
UDN2954W	12-Pin Power-Tab SIP

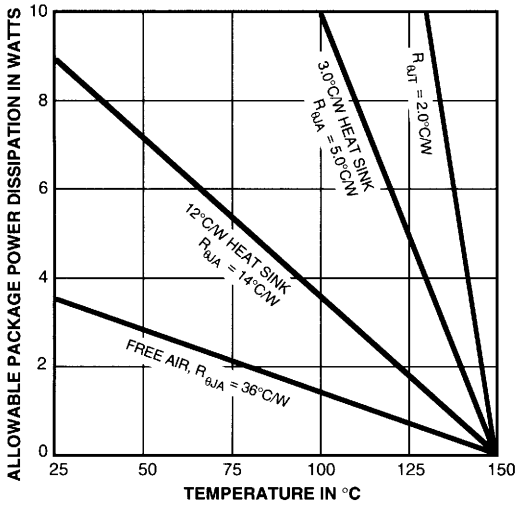
Allegro™ MicroSystems, Inc.

UDN2953B



Dwg. GP-010B

UDN2954W



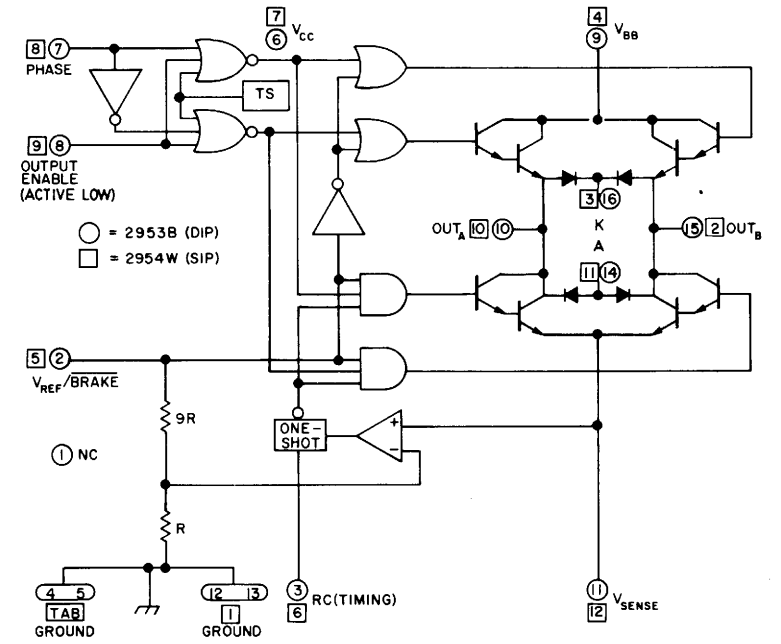
Dwg. GP-012A

TRUTH TABLE

Output Enable	Phase	V_{REF}/$\overline{BRAKE}$	Out_A	Out_B
Low	High	> 2.4 V	High	Low
Low	Low	> 2.4 V	Low	High
High	X	> 2.4 V	Open	Open
X	X	< 0.8 V	High	High

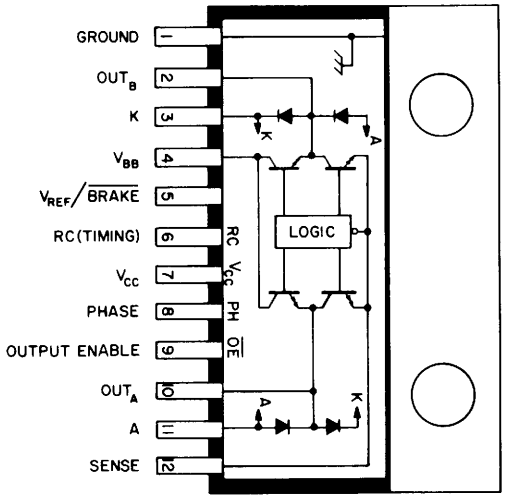
X = Irrelevant

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-13,028

UDN2954W



Dwg. No. A-13,023

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ +150°C, V_{BB} = 50 V, V_{CC} = 5 V, V_{SENSE} = 0 V, RC = 20 kΩ/470 pF to Ground.

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers (OUT_A or OUT_B)						
Output Supply Range	V_{BB}		6.5	—	50	V
Output Leakage Current	I_{CEX}	V_{ENABLE} = 5 V, V_{OUT} = V_{BB}, (note)	—	—	50	µA
		V_{ENABLE} = 5 V, V_{OUT} = 0 V, (note)	—	—	-50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±2 A, L = 2 mH	50	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	V_{ENABLE} = 0 V, I_{OUT} = ±0.5 A	—	1.0	1.2	V
		V_{ENABLE} = 0 V, I_{OUT} = ±1.0 A	—	1.2	1.4	V
		V_{ENABLE} = 0 V, I_{OUT} = ± 2.0 A	—	1.5	1.8	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 2 A	—	1.8	2.2	V
Motor Supply Current	$I_{BB(ON)}$	V_{ENABLE} = 0.8 V, V_{REF} = 2.4 V, No Load	—	20	30	mA
	$I_{BB(OFF)}$	V_{ENABLE} = V_{REF} = 2.4 V, No Load	—	2.5	3.5	mA
		V_{ENABLE} = 5 V, V_{REF} = 0.8 V, No Load	—	40	60	mA
Control Logic						
Logic Supply Range	V_{CC}		4.5	5.0	5.5	V
Logic Input Current	$I_{IN(1)}$	All Inputs = 2.4 V	—	<-1.0	-10	µA
	$I_{IN(0)}$	All Inputs = 0.8 V	—	-50	-200	µA
Logic Input Voltage	$V_{IN(1)}$	All Inputs	2.4	—	—	V
	$V_{IN(0)}$	All Inputs	—	—	0.8	V
V_{REF} Open-Circuit Voltage	$V_{REF(OPEN)}$	I_{REF} = 0	—	V_{CC}/2	—	V
Current Limit Threshold		V_{REF}/V_{SENSE} at Trip Point	9.5	10	10.5	—
Turn-On Delay	t_{on}	All Drivers	—	1.0	—	µs
Turn-Off Delay	t_{off}	All Drivers	—	1.0	—	µs
Thermal Shutdown Temp.	T_J		—	165	—	°C
Logic Supply Current	I_{CC}	V_{ENABLE} = V_{REF} = 2.4 V	—	15	20	mA
		V_{ENABLE} = 0.8 V, V_{REF} = 2.4 V	—	22	30	mA

NOTE: Tests performed at OUT_B with V_{PHASE} = 0.8 V and at OUT_A with V_{PHASE} = 2.4 V

2953 AND 2954
FULL-BRIDGE PWM MOTOR DRIVERS

APPLICATIONS INFORMATION

The UDN2953B and UDN2954W full-bridge motion control ICs are designed for pulse-width-modulated (PWM) bidirectional interface to many types of dc (brush) servo, brushless dc, and 2-phase stepper motors. These power ICs permit various techniques of direct motor interface and offer internally and externally programmed current control. Pulse-width-modulated output current can be regulated by an (external) PWM control signal or use of an external sensing resistor (R_{SENSE}) in combination with an RC network and/or voltage reference.

The output current trip point or sense resistor formulas are:

$$I_{TRIP} = \frac{V_{REF}}{10\ R_{SENSE}}$$

$$R_{SENSE} = \frac{V_{REF}}{10\ I_{TRIP}}$$

The allowable reference voltage range is from 2.4 V to 15 V. If unconnected, the reference input (V_{REF}) defaults to $V_{CC}/2$ (refer to Figure 1) and I_{TRIP} = 0.5 A (per typical application where R_S = 0.5 Ω).

When the motor current attains the specified design value, the internal comparator triggers the monostable ('one-shot') multivibrator, which disables (switches OFF) the sink (lower) output. The actual load current may vary slightly, and the difference is (chiefly) related to the circuit propagation delays between comparator (trip point) command and power output switching. Applications involving very-low inductance windings may necessitate specific consideration; typical circuit delays (t_d) are about 2 µs.

After the sink ('low-side') output is switched OFF, motor current starts to decay, and the circulation path is through the ON source (upper) drive output and the flyback diode protecting the sink (lower) output. The output OFF interval is set by an external RC timing network connected to the monostable. The magnitude of the current decay is directly related to the OFF period and the duration should allow the current level to drop below the trip point before reactivating the sink output. This ON-OFF PWM cycle repeats, sustaining the desired average current to the motor winding, and continues free-running until a new input command switches the output state. The RC network values range from 20 kΩ to 100 kΩ for resistors, and capacitor values from 200 pF to 500 pF. The parallel RC network establishes the t_{off} interval and directly affects the decaying motor current.

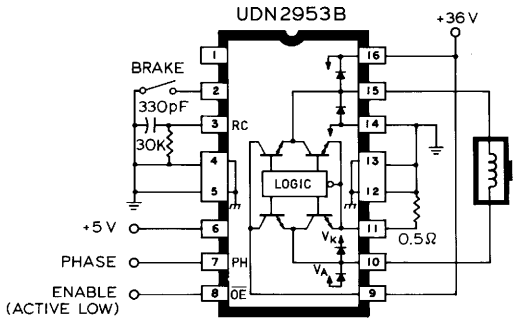
Internal timing circuitry is an alternative to the external RC timing network. However, with internal timing the logic supply current rises approximately 6 mA. Connecting the RC input to the logic supply activates internal circuitry; t_{off} = 12 µs with V_{CC} = +5 V and T_A = +25 C, and increases with temperature.

The sink (lower) output is repeatedly re-enabled until the motor is reversed, braked, or stopped. Current control via pulse modulating the lower outputs is based on the dynamic characteristics of the much faster NPN Darlington outputs.

Another method of controlling motor current involves external circuitry to pulse modulate the OUTPUT ENABLE pin. Switching (toggling) the OUTPUT ENABLE affects both the sink (low-side) and upper (high-side) outputs. Both lower and upper transient-protection diodes conduct during the OFF interval. This method of operation produces very rapid current decay. The sink driver parallel diodes (common anode pin) are connected to ground; the source output flyback diodes (common cathode pin) are connected to the motor supply (V_{BB}). The RC input pin is to be terminated to ground through 20 kΩ (minimum).

The motor is braked by simultaneously activating both source driver outputs and disabling both sink outputs. Basically, this shorts both terminals of the motor winding to the supply. The back EMF (electromotive force) of the motor develops current which functions as a dynamic brake. Typically, the braking current approaches the values related to a locked rotor (or stall) condition. Fundamentally, locked rotor (or stall) current is dependent upon the motor winding impedance and driver output ON characteristics. Internal current control circuitry is not operational during braking. Therefore, designers should exercise caution to ensure that the current produced by the back EMF does not exceed the absolute maximum ratings of the power outputs.

TYPICAL APPLICATION



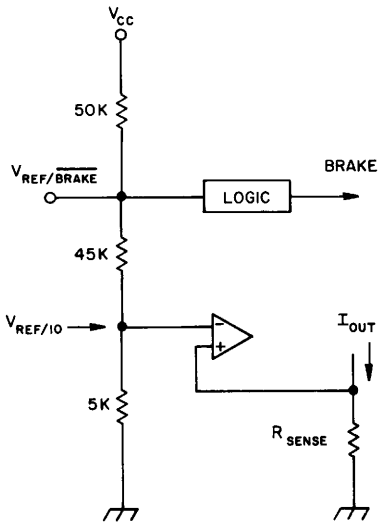
Dwg. No. A-12,649B

NOTE: Pin 3 must be connected to an RC network as shown, or to V_{CC}. It must **NOT** be left unconnected.

Allegro MicroSystems, Inc.

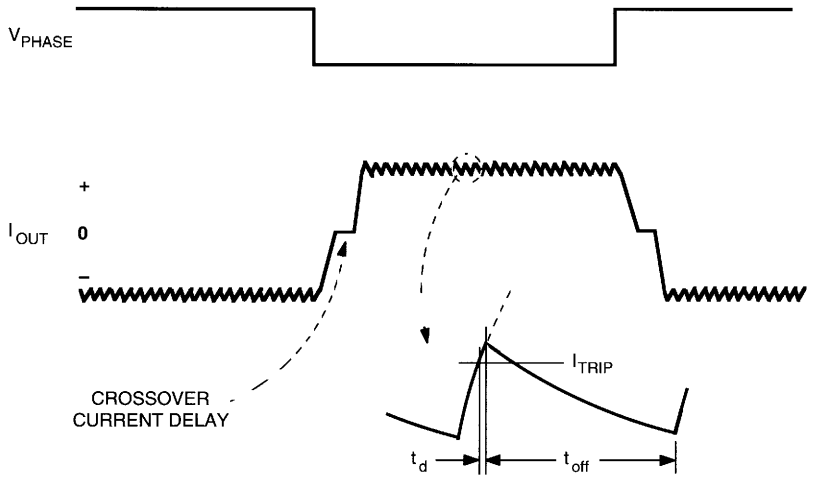
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

Figure 1



Dwg. No. A-13,025

Figure 2



Dwg. WM-003-1

In bidirectional drive applications, especially dc (brush) servos, the PHASE input is utilized for direction control. The current generated by back EMF at reversal is comparable to that of dynamic braking, and should be limited to the absolute maximum output current rating.

An internally generated deadtime (approximately 3 µs) precludes the high crossover (or 'shoot-through') currents associated with momentary, overlapping conduction of both upper and lower outputs. This very abrupt, coincident-ON mode occurs with change of direction (PHASE reversal) and/or dynamic braking.

Integrated thermal shutdown protection circuitry switches OFF all power outputs should the junction temperature exceed +165°C (typical). The thermal protection is designed to avoid power IC failures stemming from extreme, excessive junction heating. Thermal shutdown self protection does not afford a proper safeguard from shorted load and/or shorted output conditions, and should not be operated as such. The thermal self-protection circuitry has a (typical) hysteresis of 8°C.

The printed wiring board should utilize a large, heavy ground plane. To optimize power IC performance, the package should be soldered directly into the circuit board. The ground side of R_S should have an individual path to the ground terminal(s) of the device. Also, the load supply (V_{BB}) should be closely decoupled with an electrolytic capacitor of between 10 µF and 100 µF (typically ≥47 µF) depending on printed wiring board layout.

CURRENT CONTROL OPTIONS

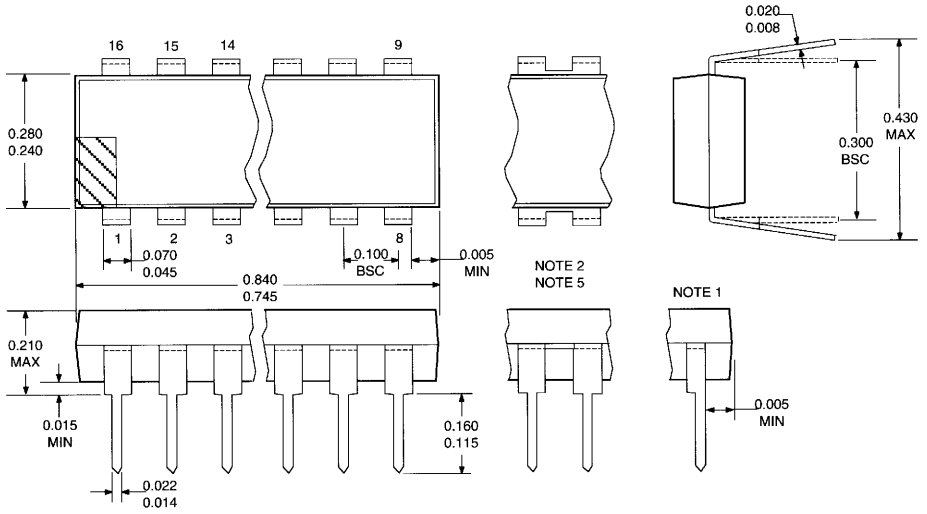
	Circuit Terminal			
Control Option	**V_{REF}/BRAKE**	**RC (TIMING)**	**V_{SENSE}**	**OUTPUT ENABLE**
No PWM	V_{CC} or High	≥20 kΩ to Ground	Ground	Low
PWM with Internal Timing	V_{CC} or High	V_{CC}	R_{SENSE}	Low
PWM with External Timing	2.4 V or 15 V* or V_{CC}	20-100 kΩ/200-500 pF	R_{SENSE}	Low
External PWM	V_{CC} or High	≥20 kΩ to Ground	R_{SENSE}†	Toggle†

* Programmed reference, i.e., A/D converter.

† Primarily, closed-loop speed and/or current control applications. I_{TRIP} can be peak (or default) limit for protecting motor and/or driver IC.

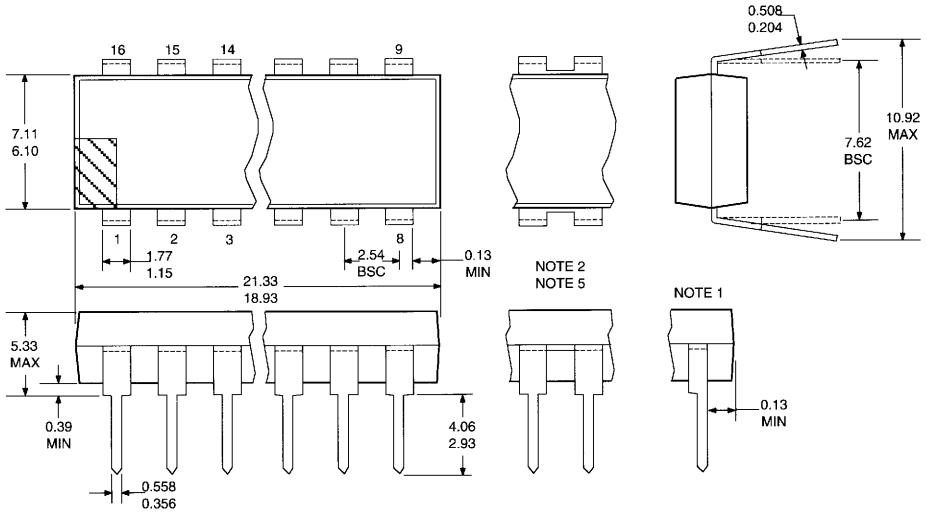
UDN2953B

Dimensions in Inches



Dwg. MA-001-17 in

Dimensions in Millimeters
(Based on 1" = 25.4 mm)



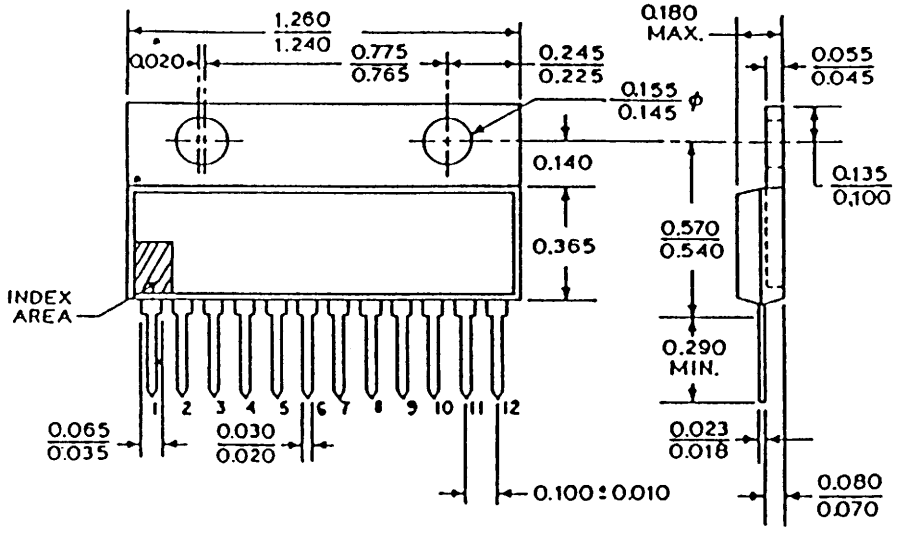
Dwg. MA-001-17 mm

NOTES:
1. Leads 1, 8, 9, and 16 may be half leads at vendor's option.
2. Webbed lead frame. Leads indicated are internally one piece.
3. Lead thickness is measured at seating plane or below.
4. Lead spacing tolerance is non-cumulative.
5. Exact body and lead configuration at vendor's option within limits shown.

Allegro™ MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

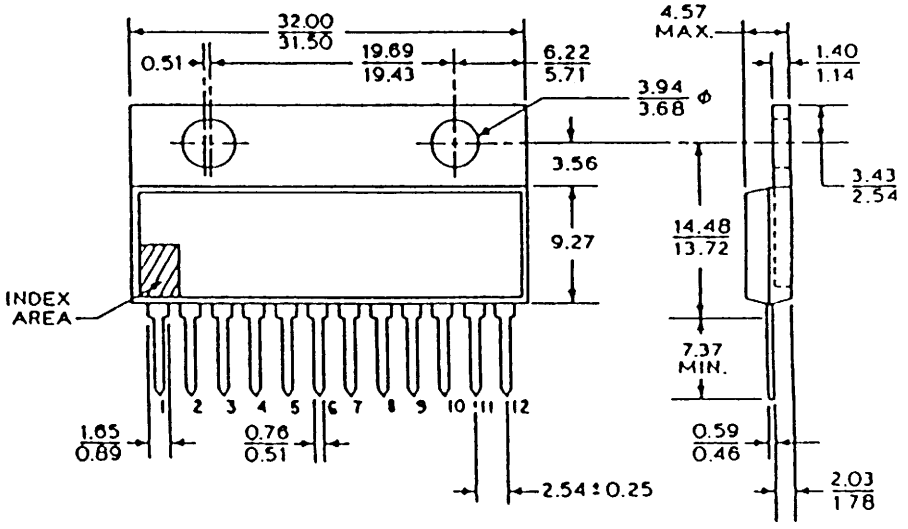
UDN2954W

Dimensions in Inches



Dwg. No. A-13,652 in

Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. No. A-13,652 mm

NOTES:
1. Lead thickness is measured at seating plane or below.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.
4. Lead gauge plane is 0.030" (0.762 mm) below seating plane.