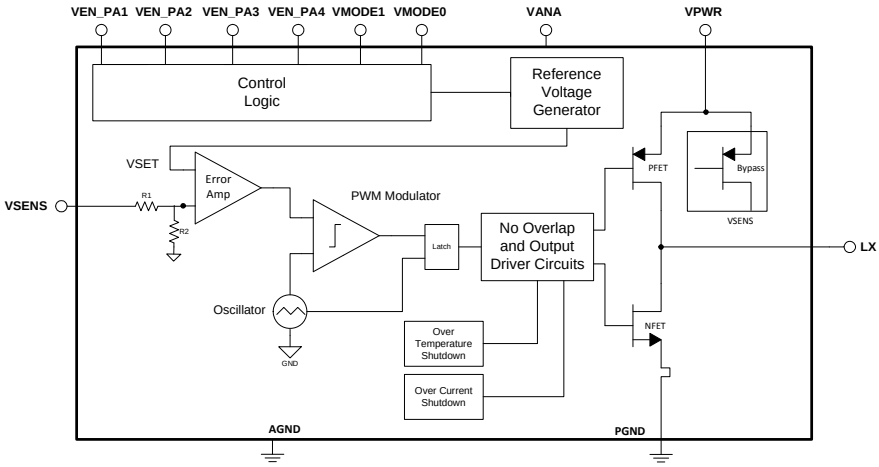
Package: 12-Bump WLSCP, 4 x 3 Array 1.65mm x 1.25mm

Features

- Digital Mode Control Compatibility
- Provides the PA biasing for Three Power Modes (HP, MP, LP)
- Optimum Performance with RFMD's High Efficiency PA products
- Interface to Multiple PA(s)
- Optimized Maximum V_{CC} at 3.4V
- High Efficiency >94%
- Transient Response <25µs
- 650mA Load Current Capability
- V_{BAT} Range = 2.7V to 5.0V
- Automatic Bypass Mode
- Over-Temperature Shutdown
- Over-Current Shutdown

Applications

- WCDMA Handsets
- CDMA Handsets
- UMTS Datacards



Functional Block Diagram

Product Description

The RF6652 is a pulse width modulated (PWM), discrete voltage-mode controlled DC-DC converter unit designed to supply power to a WCDMA power amplifier. The output voltage can be programmed by two control logic inputs to select the power mode for the PA. The DC-DC converter has been optimized for high efficiency at light current load conditions when PA is in low power mode. The RF6652 DC-DC PMIC offers fast transient response times to meet WCDMA 25µs slot-to-slot transition specifications and low noise by maintaining a constant switching frequency while supplying up to 650mA in PWM mode. The RF6652 is enabled when the PA enables (V_{EN} >1.3V) and V_{MODE0} and V_{MODE1} are used to select the V_{CC} to be supplied to the PA for each power mode. The RF6652 is a 1.65mm x 1.25mm, 12-bump, WLSCP device.

Ordering Information

RF6652	Power Management IC
RF665299PCBA-410	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ BiFET HBT
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Input Supply Voltage	-0.2 to +5.0	V
Analog/Digital Inputs (VEN_DC, VMODE0, VMODE1, VEN_PA1, VEN_PA2, VEN_PA3, VEN_PA4	-0.2 to V_{ANA}+0.2	V
Ground Voltage	-0.2 to +0.2	V
Operating Ambient Temperature	-30 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Operating Conditions					
Supply Voltage	2.7	3.6	5.0	V	
Output Load Current			650	mA	
Junction Temperature	-30		+125	°C	
Operating Temperature	-30		+85	°C	
General Specifications					
Quiescent Current		700	1400	µA	Internal V_{SET} = 0V, no load
Shut Down Current			10	µA	V_{EN_PA1} = V_{EN_PA2} = V_{EN_PA3} = V_{EN_PA4} = 0V
Logic High Input Threshold	1.3			V	V_{EN_DC}, V_{MODE0}, V_{MODE1}, V_{EN_PA1}, V_{EN_PA2}, V_{EN_PA3}, V_{EN_PA4}
Logic Low Input Threshold			0.5	V	
Input Current			1.0	µA	Max current on any logic pin
Thermal Shutdown		150		°C	Rising Temperature
		130		°C	Falling Temperature
		20		°C	Hysteresis
Over-Current Shutdown Trip Points		2.4		A	Full FET, V_{OUT} = 3.4V
		1.6		A	1/3 FET, V_{OUT} = 0.8V
DC Specifications					
V_{OUT}		3.40		V	V_{MODE0} = 0, V_{MODE1} = 0
		1.06		V	V_{MODE0} = 1, V_{MODE1} = 0
		0.65		V	V_{MODE0} = 1, V_{MODE1} = 1
V_{OUT} Error			2.0	%	All modes, V_{BAT} = 3.4V to 4.8V
Efficiency		66		%	V_{OUT} = 0.8V, I_{OUT} = 20mA
		85		%	V_{OUT} = 0.8V, I_{OUT} = 60mA
		92		%	V_{OUT} = 1.40V, I_{OUT} = 200mA
		94		%	V_{OUT} = 3.4V, I_{OUT} = 550mA
Output Voltage Ripple		15		mVpp	MPM, V_{OUT} = 1.49V
Dropout Voltage		170		mV	HPM, V_{BAT} = 3.4V, I_{OUT} = 500mA , (R_{ESRL} = 100mΩ), V_{DO} = V_{BAT} - V_{OUT}
Load Regulation			20	mV/A	Low Power Mode, V_{OUT} = 0.8V, I_{OUT} = 20mA to 60mA
			20	mV/A	Medium Power Mode, V_{OUT} = 1.49V, I_{OUT} = 60mA to 200mA
			20	mV/A	High Power Mode, V_{OUT} = 3.4 V, I_{OUT} = 400mA to 550mA

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DC Specifications (continued)					
Line Regulation			10	mV/A	Low Power Mode, V_{OUT} = 0.8V, I_{OUT} = 25mA, V_{BAT} = 3.3V to 3.9V
			10	mV/A	Medium Power Mode, V_{OUT} = 1.49V, I_{OUT} = 60mA, V_{BAT} = 3.3V to 3.9V
			10	mV/A	High Power Mode, V_{OUT} = 3.4V, I_{OUT} = 450mA, V_{BAT} = 3.6V to 4.2V
AC Specifications					
Switching Frequency		2		MHz	Over V_{BAT} and temperature
V_{OUT} Startup Time		12	35	µS	V_{OUT} = 0V to 0.6V ±10%, I_{OUT} < 1mA
		6	35	µS	V_{OUT} = 0V to 3.4V ±10%, I_{OUT} < 1mA, $V_{BAT} \geq$ 4.2V
V_{OUT} Response Time		8	25	µS	V_{OUT} = 0.6V to 3.4V ±100mV, R_{LOAD} = 5Ω, $V_{BAT} \geq$ 4.2V
		9	30	µS	V_{OUT} = 3.4V to 0.6V ±100mV, R_{LOAD} = 25Ω, $V_{BAT} \geq$ 4.2V
SMPS to BYPASS Time		1.5	5	µS	MPM to HPM, I_{OUT} = 460 mA, V_{BAT} = 3.0V
		4	20	µS	V_{BAT} = 4.6V to 3.0V, I_{OUT} = 460mA, HPM
BYPASS to SMPS Time		40	50	µS	HPM to MPM, I_{OUT} = 460mA, V_{BAT} = 3.0V
		10	50	µS	V_{BAT} = 3.0V to 4.6V, I_{OUT} = 460 mA, HPM
Load Transient		30	100	mVpk	V_{OUT} = 600mV, I_{OUT} = 20mA to 200mA, T_{RISE} = T_{FALL} = 10µs
		16	50	mVpk	V_{OUT} = 3.4V, I_{OUT} = 400mA to 550mA, V_{BAT} = 4.2V
Line Transient		30	35	mVpk	V_{OUT} = 600mV, I_{OUT} = 60mA, ΔV_{BAT} = 600mV, T_{RISE} = T_{FALL} = 10µs
		135	150	mVpk	V_{OUT} = 3.4V, I_{OUT} = 450mA, ΔV_{BAT} = 600mV, T_{RISE} = T_{FALL} = 10µs, V_{BAT} = 4.2V
Bypass Specifications					
Resistance		140	200	mΩ	V_{BAT} = 3.0V, I_{OUT} = 500mA (net resistance)
Enable Trip Point (V_{BAT})		3.5		V	Falling V_{BAT}, I_{OUT} = 500mA, HPM
Disable Trip Point (V_{BAT})		3.7		V	Raising V_{BAT}, I_{OUT} = 500mA, HPM
Dropout Voltage			100	mV	V_{BAT} = 3.0V, I_{OUT} = 500mA, Dropout = V_{BAT} - V_{OUT}
V_{OUT} Startup Time		4	15	µS	V_{BAT} = 3.0V. $I_{OUT} \leq$ 1mA

V_{OUT} Values for all Four VEN_PAx Selections

(These Values are Factory Set for the RF6652)

V_{OUT} Values for each Mode	VEN_PA1	VEN_PA2	VEN_PA3	VEN_PA4
High Power Mode	3.4V	3.4V	3.4V	3.4V
Medium Power Mode	1.48V	1.48V	1.36V	1.36V
Low Power Mode	0.84V	0.84V	0.78V	0.76V

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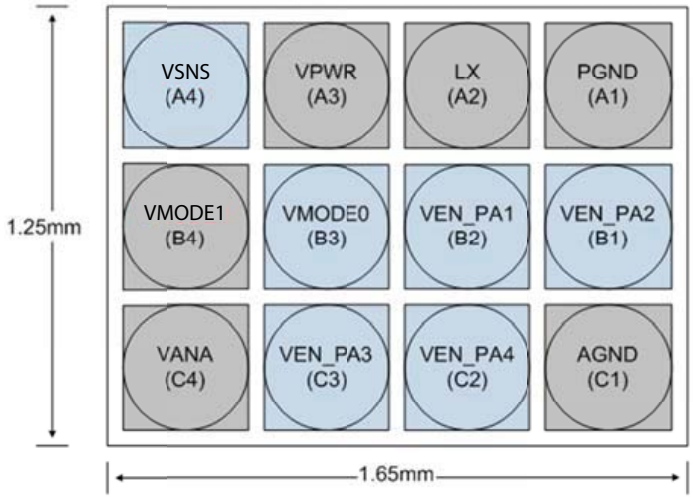
Pin Names and Descriptions

Pin	Name	Description
A1	PGND	DC-DC Converter Power Ground
A2	LX	DC-DC Converter Switcher Output. Connect to the filter inductor as recommended on application schematics. Provides three set voltages to correspond to HP, MP, and LP modes for the PA.
A3	VPWR	Supply used for the DC-DC PFET switch. A 2.2 μF decoupling capacitor is required on this pin
A4	VSNS	Feedback node from the output of the external LC filter. Connect at a point after the VOUT inductor and/or near the PA VCC pin.
B1	VEN_PA2	Logic level that selects a specific internal PA biasing levels for LP, MP, and HP modes.
B2	VEN_PA1	Logic level that selects a specific internal PA biasing levels for LP, MP, and HP modes.
B3	VMODE0	Logic level that selects the power mode (HP, MP, or LP mode)
B4	VMODE1	Logic level that selects the power mode (HP, MP, or LP mode)
C1	AGND	Ground for the analog circuits. Isolate from the PGND to better reduce noise.
C2	VEN_PA4	Logic level that selects a specific internal PA biasing levels for LP, MP, and HP modes.
C3	VEN_PA3	Logic level that selects a specific internal PA biasing levels for LP, MP, and HP modes.
C4	VANA	Supply used for the analog circuitry inside the RF6652 power management IC. A 2.2 μF decoupling capacitor is required.

Pin Out

QB Single-Ended (Bottom View)



Note: VEN_PA4 will be treated as VEN_DC in the configuration with three (3) PAs and a seperate DC-DC Enable.

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Theory of Operation

DC-DC buck converter operation involves the stepping down of a higher battery voltage to a lower output voltage by alternately switching a PFET and NFET pair through an external LC filter. At a 2MHz switching frequency the PFET is enabled every 500ns. Based on the power mode of the PA, an accurate internal reference voltage V_{SET} is set up. The duty cycle at the Lx switching node, which is continuously variable from 0% to 100%, is set by the PWM controller based on internal V_{SET} and V_{BAT} voltages to realize the desired output voltage. The PWM controller maintains accuracy, stability, and accounts for losses in the system by feedback through the VSENS pin. The controller has been designed with non-overlapping control circuitry to prevent V_{BAT} overshoot-through current to ground.

The converter has been optimized for high efficiency at light load by balancing DC and AC switching losses incurred in the output FETs, the switching frequency, and the external LC filter. In addition, output FET segmentation and selective biasing have been employed to further enhance light load efficiencies.

Unlike other DC-DC converter solutions on the market, the RF6652 does not alter the switching frequency at light load conditions to boost efficiency. This type of efficiency enhancement has a severe detriment on the system by injecting spurious noise at various frequencies. With our expertise in front end transmit module design, RFMD proposes to operate this converter at a constant switching frequency to minimize system level interference. The ripple voltage, also a major component of noise injection into the PA, has also been minimized by selecting a larger inductance value.

Despite the attention to high efficiency, the transient performance of the device, defined as an output voltage transient from 600mV to 3.4V or vice-versa, has not been overlooked. The PWM controller has been properly tuned with a fast type III loop filter to mate with an external LC filter (L = 2.2μH and C = 2.2μF + 1μF + 1μF = 4.2μF). The result is a converter with sufficient bandwidth to meet 25μs WCDMA slot-to-slot transition time requirements.

(Note: If four PA(s) are used then a 0.47μF can be placed at each of the four PA VCC pins. If only two PA(s) are used, then a 1μF can be at both PA VCC pins.

Lastly, the external inductor and capacitors were specifically selected to balance efficiency over the load current operating range and transient performance while minimizing total board area. Inductors and capacitors of different values may be used at risk to DC-DC converter stability and efficiency performance.

Control Interface

The V_{MODE0} and V_{MODE1} will adjust what power mode the PA will be in and load condition of the RF6652.

Input Logic Table to provide PA power mode control

VMODE0	VMODE1	PA Mode
0	0	High Power
1	0	Medium Power
1	1	Low Power

Shutdown

The shutdown mode is determined by the following logic table:

VEN_PA1	VEN_PA2	VEN_PA3	VEN_PA4	VMODE1	VMODE0
0	0	0	0	X	X
X = “Don’t Care” Condition					

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Over-Temperature Protection

An internal over-temperature shutdown circuit is employed to protect the device from excessively high junction temperatures. The shutdown occurs at typically 150°C and will re-enable when the temperature drops below the activation point typically by 20°C.

Over-Current Protection

For the RF6652, an over-current shutdown (OCSD) circuit is employed to provide over-current fault protection. This methodology deactivates the output FETs in the case of an over-current fault as opposed to limiting the current. In this way the device only experiences the over-current condition for a short transient period and is not subject to continuous high current flow. Once the DUT is shut down, it will not restart automatically if the fault condition is removed.

Bypass Mode

RF6652 contains an automatic bypass mode that activates a large PFET device in parallel with the SMPS PFET when there is insufficient headroom available between V_{BAT} and the desired output voltage. This mode is enabled when there is less than 100mV of headroom available and is disabled when the available headroom increases above 300mV. The bypass FET reduces the output resistance and dropout voltage at high power mode.

FET Segmentation

The main power FETs are designed in three sections to improve efficiency during light load conditions expected with low output voltages. In medium and high power modes, all three sections of the output FETs are on (full FET mode). When the part operates in low power mode, only one of the three sections is used (1/3 FET mode).

Board Layout

Good DC-DC converter layout practices in this application are strongly recommended to reduce radiated and conducted system noise. Placement of the VPWR bypass capacitor is critical and must be such to minimize the AC supply and ground return current loop through the PFET. In addition, the placements of the LC filter (L1 and C1) are also critical to minimize the AC supply and ground return current loop through the NFET.

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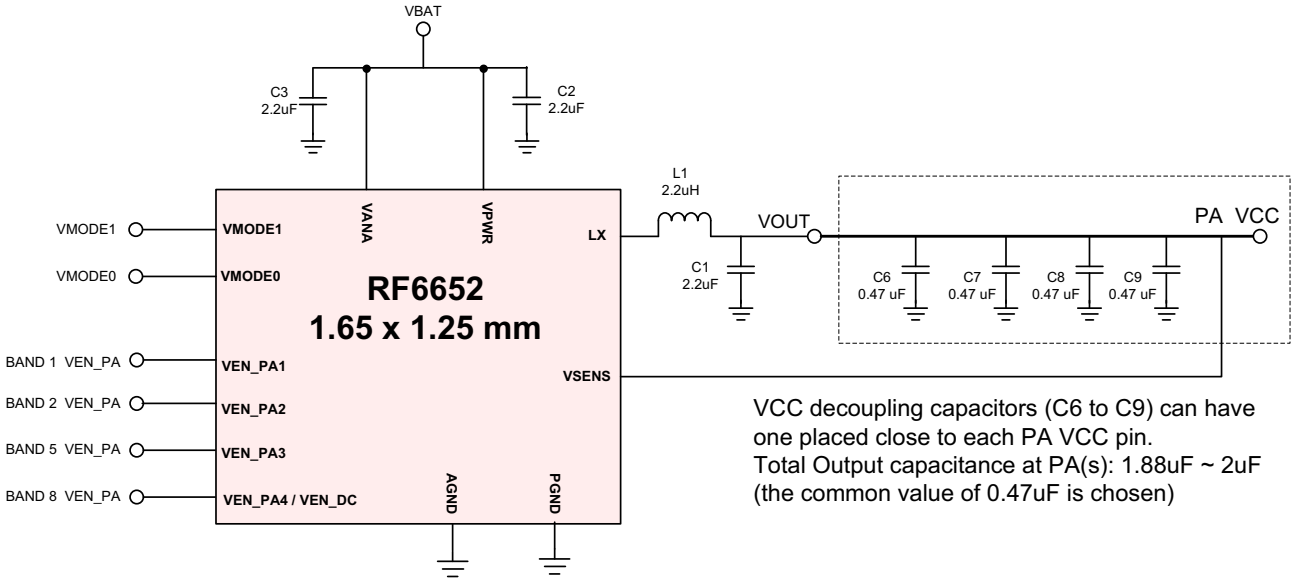
Application Schematic



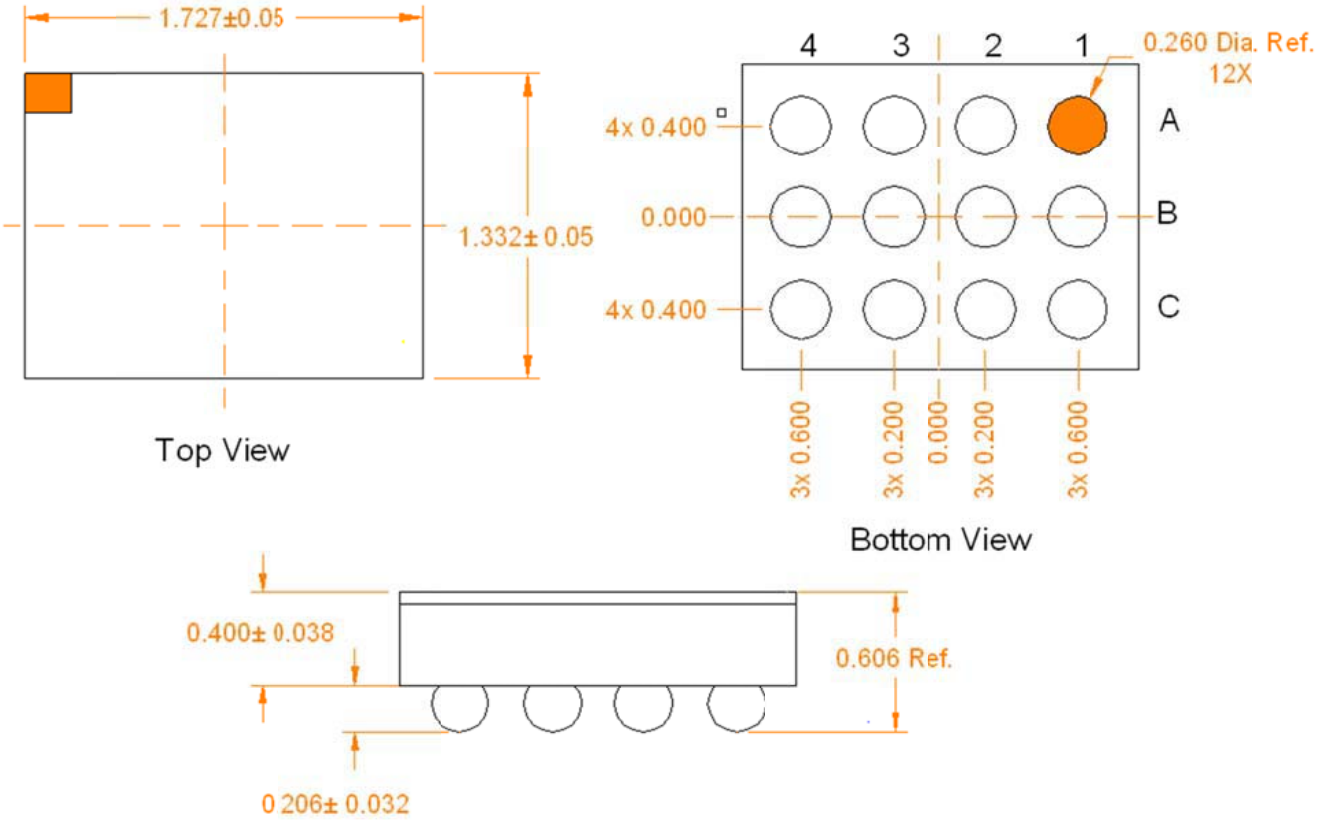
Notes: RF6652 and PA Application with related EVB components:

1. The LC filter (power filter) consists of L1 and C1 near the RF6652 and the distributed capacitances C6 thru C9 near load (PA)s. The main loop of L1 and C1 should be as small as possible with a large ground plane connecting C1 to the PGND pin. Capacitors C6, C7, C8, C9 are placed at the VCC pins of the loads (each PA V_{CC}) and should also have a clear return path to PGND. The loop filter is designed to have a total capacitance of 4.2µF (C1 = 2.2µF + 1µF + 1µF) or equal to (C1 = 2.2µF + 4 x (0.47µF). This would be the configuration for four PA(s).
2. Capacitors C2 and C3 are placed a small distance away from the DUT on the evaluation board to emulate the distributed effects of the trace resistance as would be expected in the application.
3. A separate decoupling capacitor should be used for the VPWR and VANA pins. The current return path for the analog and power sections should be kept separate to decrease the number of component types, a value of 2.2µF is selected.
4. The parasitic resistance of L1 and C1 should be kept within the limits RESRL<100mΩ, R_{ESRC} = 10mΩ. Recommended components are given in the table below. Selecting alternate components will have an impact on the reported performance including, but not limited to, changes in the efficiency.

Application Schematic and Related EVB Components

Designator	Case Size	Quantity	Manufacturer	Value	Part Number
L1	2.5 X 2.0 X 1.0	1	2.2µH	Murata	LQM2HPN2R2MG0L
C1	0603	1	2.2µF	Murata	GRM188R61A225KE34D
C2, C3	0603	2	1µF	Taiyo Yuden	RMTMK107BJ105KA-T

Package Drawing



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