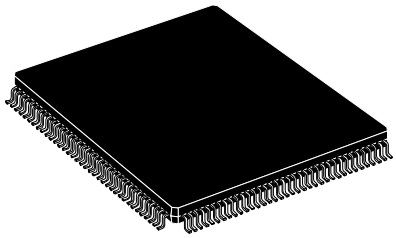
ST10F276, ST10F273

16-bit MCU with MAC unit, up to 832 Kbytes Flash memory and up to 68 Kbytes RAM

DATA BRIEF

- **High performance 64 MHz CPU with DSP functions**
  - 16-bit CPU with 4-stage pipeline
  - 31.25ns instruction cycle time at 64 MHz max. CPU clock
  - Multiply/accumulate unit (MAC) 16 x 16-bit multiplication, 40-bit accumulator
  - Repeat unit
  - Enhanced boolean bit manipulation facilities
  - Additional instructions to support HLL and operating systems
  - Single-cycle context switching support
- **Memory organization**
  - 512 Kbytes on-chip flash memory single voltage with erase/program controller (full performance, 32-bit fetch)
  - Up to 320 Kbytes on-chip extension flash memory single voltage with erase/program controller (XBUS performance, 16-bit fetch)
  - 100K erasing/programming cycles.
  - Up to 16 Mbytes linear address space for code and data (5m bytes with CAN or I^2C)
  - 2 Kbytes on-chip internal RAM (IRAM)
  - Up to 66 Kbytes on-chip extension RAM (XRAM)
- **Fast and flexible bus**
  - Programmable external bus characteristics for different address ranges
  - 8-bit or 16-bit external data bus
  - Multiplexed or demultiplexed external address/data buses
  - Five programmable chip-select signals
  - Hold-acknowledge bus arbitration support
- **Interrupt**
  - 8-Channel peripheral event controller for single cycle interrupt driven data transfer
  - 16-Priority-level interrupt system with 56 sources, sampling rate down to 15.6ns
- **Timers**
  - Two multi-functional general purpose timer units with 5 timers



PQFP144 (28 x 28 x 3.4mm)
TQFP144 (20 x 20 x 1.4mm)

- **Two 16-channel capture / compare units**
- **A/D converter**
  - 24 channels with 10-bit resolution
  - 3µs minimum conversion time
- **4-channel PWM unit + 4-channel XPWM**
- **Serial channels**
  - Two synch. / asynch. serial channels
  - Two high-speed synchronous channels
  - I^2C standard interface
  - Two CAN 2.0B interfaces operating on one or two CAN busses (64 or 2x32 message objects, C-CAN version)
- **Fail-safe protection**
  - Programmable watchdog timer
  - Oscillator watchdog
- **On-chip bootstrap loader**
- **Clock generation**
  - On-chip 4-12 MHz main oscillator
  - On-chip PLL
  - Direct or prescaled clock input
- **Real time clock and 32 kHz on-chip oscillator**
- **Up to 111 general purpose I/O lines**
  - Individually programmable as input, output or special function
  - Programmable threshold (hysteresis)
  - Idle, Power down and Stand-by modes
  - Single voltage supply: 5V ±10% (embedded regulator for 1.8V core supply)

1 Ordering information

Table 1. Ordering information

Part Number	Iflash	Xflash	RAM	Temperature range	Package
ST10F276Z5Q3	512KB	320KB	68KB	40/+125	PQFP144
ST10F276Z5T3	512KB	320KB	68KB	40/+125	TQFP144
ST10F273Z4Q3	512KB	No	32KB	40/+125	PQFP144
ST10F273Z4T3	512KB	No	32KB	40/+125	TQFP144

1.1 ST10F276/ST10F273 compatibility

The only differences between ST10F276 and ST10F273 devices are the embedded Flash and RAM resources:

Flash Memory: ST10F276 includes 832 Kbytes of on-chip single voltage Flash divided into four banks allowing for Read-While-Write Operation. Two banks are mapped on the internal 32-bit bus (IFLASH) and the two others are mapped on 16-bit XBUS (XFLASH).

- In ST10F273 devices the XFLASH banks are not available. As a consequence, only the standard ST10 bootstrap mode can be used (no Alternate Boot Mode).

RAM: The ST10F273 includes 68 Kbytes of on-chip RAM, divided into 3 blocks: 2 Kbytes IRAM dual-ported RAM block, 2 Kbytes XRAM1 extension RAM block and 64KBytes XRAM2 extension RAM block.

- In ST10F273 devices the XRAM2 on-chip extension RAM block is reduced to 32 Kbytes.

Note: There is no built-in feature to allow software to detect if the device is an F276 or an F273. The missing memory in the ST10F273 can be seen as regular memory. If you wish make two assemblies of the same PCB with the ST10F276 and ST10F276, we advise to put a pull-up resistor on an I/O to differentiate the two configurations by software.

Table 2. XFLASH Blocks User Mode Size

Block	Address	ST10F276	ST10F273
B2F0	09'0000h - 09'FFFFh	64KB	Reserved
B2F1	0A'0000h - 0A'FFFFh	64KB	Reserved
B2F2	0B'0000h - 0B'FFFFh	64KB	Reserved
B3F0	0C'0000h - 0C'FFFFh	64KB	Reserved
B3F1	0D'0000h - 0D'FFFFh	64KB	Reserved
CTRL Registers	0E'0000h - 0E'FFFFh	64KB	Reserved

Table 3. XRAM Blocks User Mode Size

Block	Address	ST10F276	ST10F273
XRAM1 - 2KB	00'E000h - 00'E7FFh	2KB	2KB
XRAM2 - Standby RAM - 16KB	0F'0000h - 0F'3FFFh	16KB	16KB
XRAM2 - Following 16KB	0F'4000h - 0F'7FFh	16KB	16KB
XRAM2 - Following 32KB	0F'8000h - 0F'FFFFh	32KB	reserved

2 Related documents

This document provides the ST10F276 and ST10F273 ordering information, for detailed technical specifications, please refer to the ST10F276 Datasheet and User's Manual.

3 Revision history

Date	Revision	Changes
18-Jul-2005	1	Initial release