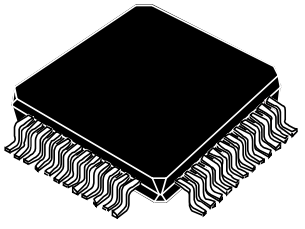
ST72681

USB 2.0 HIGH-SPEED 8-BIT MCU FLASH DRIVE CONTROLLER

PRELIMINARY DATA

- **USB 2.0 Interface compatible with Mass Storage Device Class**
  - Integrated USB 2.0 PHY
  - Supports USB High Speed and Full Speed
  - Suspend and Resume operations
- **Mass Storage Controller Interface (MSCI)**
  - Supports all type of NAND Flash devices
  - Reed-Solomon Encoder/Decoder for MLC NAND Flash support: on-the-fly correction (4 bytes of a 512-byte block)
  - Flash identification support
  - 10MB/s for read and 8MB/s for write operations with one single NAND Flash device
  - 10MB/s for read and 10MB/s for write operations in multi mode NAND Flash device topology
- **Embedded ST7 8-bit MCU**
- **Supply Management**
  - 3.3V operation
  - Integrated 3.3V-1.8V voltage regulator
- **Very low power consumption**
  - Less than 100mA during write operation with two NAND Flash devices
  - Less than 500µA in suspend mode
- **Clock Management**
  - Integrated PLL for generating core and USB 2.0 clock sources using an external 12 MHz crystal
- **Up to two configurable LED outputs**
  - Blinking on USB specific activity (idle, suspend, data access)



TQFP48

- **Data Protection**
  - Write protect switch control
  - Password-based security for data protection
- **Bootability support**
- **Flexibility**
  - Configurable Vendor ID/Product ID (VID/PID) with production tool
  - Patch code support with external EEPROM device
- **TQFP48 7x7 lead-free package**
- **Development Support**
  - Complete reference design including schematics, BOM and gerber files
- **Supports Windows ME, Windows 2K, Windows XP, Linux and MacOS. Drivers available for Windows 98 SE**

Features	ST72681
USB interface	USB 2.0
# of NAND devices supported	up to 4
R/W speed	10MBps/8MBps (single NAND) / 10MBps/10MBps (multi NAND)
Operating Supply	3.0V to 3.6V
Operating Temperature	0°C to +70°C
Packages	TQFP48 7x7 / Die form

Rev. 1.1

1 INTRODUCTION

The ST72681 is a USB 2.0 high-speed Flash Drive controller. The USB 2.0 high-speed interface including PHY and function supports USB 2.0 Mass Storage Device Class.

The Mass Storage Controller Interface combined with the Reed-Solomon Encoder/Decoder on-the-fly correction (4-byte on 512-byte data blocks) provides a flexible, high transfer rate solution for interfacing a wide of range NAND Flash memory device types.

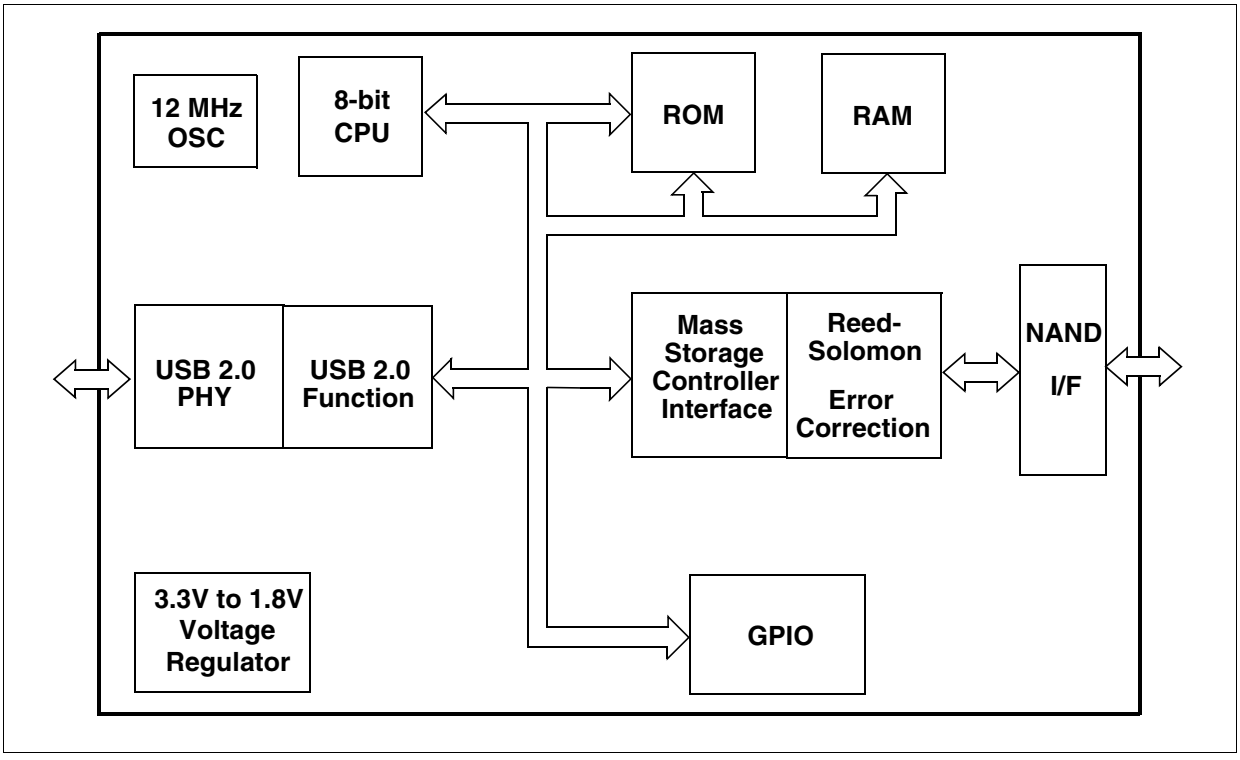
The internal 60 MHz PLL driven by the 12MHz oscillator is used to generate the 480MHz frequency for the USB 2.0 PHY.

The ST7 8-bit CPU runs the application program from the internal ROM and RAM. USB data and patch code are stored in internal RAM.

I/O ports provide functions for EEPROM connection, LEDs and write protect switch control.

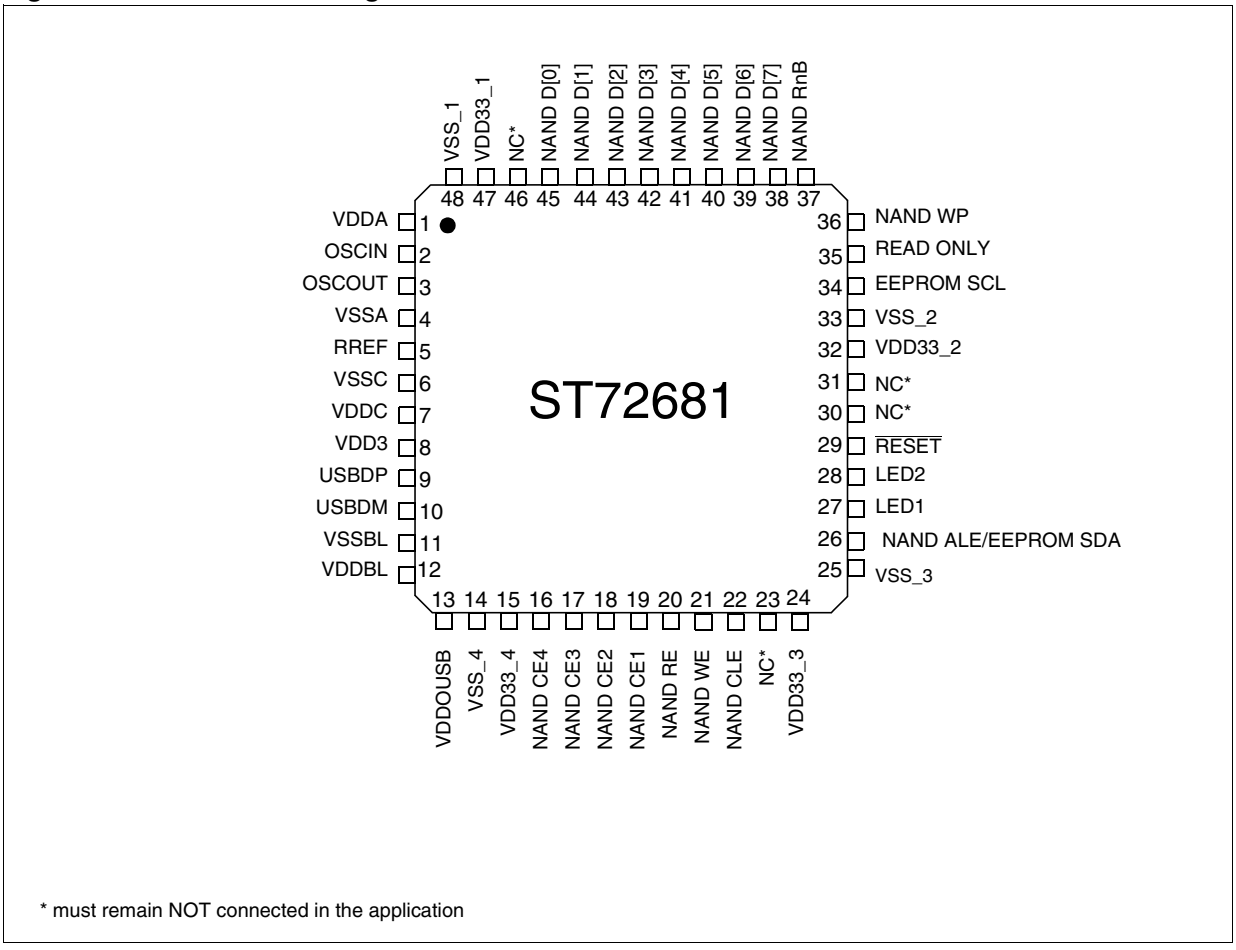
The internal 3.3V to 1.8V voltage regulator provides the 1.8V supply voltage to the digital part of the circuit.

Figure 1. Device Block Diagram



2 PIN DESCRIPTION

Figure 2. 48-Pin TQFP Package Pinout



* must remain NOT connected in the application

PIN DESCRIPTION (Cont'd)

Legend / Abbreviations for tables:

Type: I = input, O = output, S = supply

Input level: A = Dedicated analog input

In/Output level: C_T = CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

T_T= TTL 0.8V / 2V with Schmitt trigger

Output level: D8 = 8mA drive

D4 = 4mA drive

D2 = 2mA drive

Port and control configuration:

– Input: float = floating, wpu = weak pull-up, wpd = weak pull-down, int = interrupt

– Output: OD = pseudo open drain, PP = push-pull

The RESET configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

Table 1. Power Supply

Pin	Pin Name	Type	Description
48	VSS_1	S	Ground
47	VDD33_1	S	IOs and Regulator supply voltage
33	VSS_2	S	Ground
32	VDD33_2	S	IOs and Regulator supply voltage
25	VSS_3	S	Ground
24	VDD33_3	S	IOs and Regulator supply voltage
14	VSS_4	S	Ground
15	VDD33_4	S	IOs and Regulator supply voltage
13	VDDOUSB	S	USB2 PHY, OSC and PLL power supply output (1.8V)

Table 2. Control & System

Pin	Pin Name	Type	Power	Level		Description
TQFP48				Input	Output	
29	$\overline{\text{RESET}}$	I/O	3.3	C_T		Reset input with filter with internal pull-up

PIN DESCRIPTION (Cont'd)

Table 3. USB 2.0 Interface

Pin TQFP48	Pin Name	Type	Description
12	VDDBL	S	Supply voltage for buffers and deserialisation flip flops (1.8V)
11	VSSBL	S	Ground for buffers and deserialisation flip flops (1.8V)
10	USBDM	I/O	USB2 DATA -
9	USBDP	I/O	USB2 DATA +
8	VDD3	S	Supply voltage for the FS compliance (3.3V)
7	VDDC	S	Supply voltage for DLL & xor tree (1.8V)
6	VSSC	S	Ground for DLL & XOR tree (1.8V)
5	RREF	I/O	Ref. resistor for integrated impedance process adaptation (11.3 kOhms 1% Pull Down)

Table 4. USB 2.0 and core Clock System

Pin TQFP48	Pin Name	Type	Description
4	VSSA	S	Ground for osc & PLL (1.8V)
3	OSCOUT	O	12MHz oscillator output
2	OSCIN	I	12MHz oscillator input
1	VDDA	S	Supply voltage for osc & PLL (1.8V)

PIN DESCRIPTION (Cont'd)

Table 5. General Purpose IO Ports / Mass Storage IOs

Pin	Pin Name	Type	Level		Main function (after reset)	Alternate function
TQFP48			Input	Outputs		
45	NAND D[0]	I/O	T_T	D4	NAND DATA [0]	
44	NAND D[1]	I/O	T_T	D4	NAND DATA [1]	
43	NAND D[2]	I/O	T_T	D4	NAND DATA [2]	
42	NAND D[3]	I/O	T_T	D4	NAND DATA [3]	
41	NAND D[4]	I/O	T_T	D4	NAND DATA [4]	
40	NAND D[5]	I/O	T_T	D4	NAND DATA [5]	
39	NAND D[6]	I/O	T_T	D4	NAND DATA [6]	
38	NAND D[7]	I/O	T_T	D4	NAND DATA [7]	
26	NAND ALE / EEPROM SDA	I/O	T_T	D8	NAND ADDRESS LATCH ENABLE	EEPROM SERIAL DATA
22	NAND CLE	O	T_T	D8	NAND COMMAND LATCH ENABLE	
21	NAND WE	O	T_T	D8	NAND WRITE ENABLE	
20	NAND RE	O	T_T	D8	NAND READ ENABLE	
19	NAND CE1	O	T_T	D4	NAND ENABLE 1	
18	NAND CE2	O	T_T	D4	NAND ENABLE 2	
17	NAND CE3	O	T_T	D4	NAND ENABLE 3	
16	NAND CE4	O	T_T	D4	NAND ENABLE 4	
37	NAND RnB	I	T_T	D2	NAND READY/$\overline{\text{BUSY}}$	
36	NAND WP	O	T_T	D2	NAND WRITE PROTECT	
35	READ ONLY	I	T_T	D2	READ ONLY SWITCH	
34	EEPROM SCL	O	T_T	D2	EEPROM SERIAL CLOCK	
28	LED2	O	T_T	D8	GREEN LED (USB ACCESS)	
27	LED1	O	T_T	D8	RED LED (NAND ACCESS)	

3 NAND FLASH DEVICE SUPPORT

Type	Memory size	Program Page Size (in Bytes)
Samsung K9F2808U0C-Y	16M x 8b	528
Samsung K9F5608U0C-Y	32M x 8b	528
Samsung K9F1208U0A-Y	64M x 8b	528
Toshiba TC58512FT	64M x 8b	528
Toshiba TC58DVM92A	64M x 8b	528
Toshiba TC58DVG02A	128M x 8b	528
Toshiba TC58DVG04B1FT00	128M x 8b	528
Toshiba TC58DVG14B1FT00	256M x 8b	528
ST NAND128W3A	16M x 8b	528
ST NAND256W3A	32M x 8b	528
ST NAND512W3A	64M x 8b	528
ST NAND01GW3A	128M x 8b	528
Hynix HY27US08281M	16M x 8b	528
Hynix HY27US08561M	32M x 8b	528
Hynix HY27US08121M	64M x 8b	528
Samsung K9F1G08U0M-Y	128M x 8b	2112
Samsung K9F2G08U0M-Y	256M x 8b	2112
Samsung K9K2G08U0M-Y	256M x 8b	2112
Samsung K9K4G08U0M-Y	512M x 8b	2112
Samsung K9W4G08U1	512M x 8b	2112
Samsung K9W8G08U1	1G x 8b	2112
Toshiba TH58NVG0S3	128M x 8b	2112
Toshiba TH58NVG1S3	256M x 8b	2112
Toshiba TH58NVG2S3	512M x 8b	2112
ST NAND01GW3B	128M x 8b	2112
ST NAND02GW3B	256M x 8b	2112
Hynix HY27UA081G1M	128M x 8b	2112
Micron 29F2G08AA	256M x 8b	2112

4 APPLICATION SCHEMATICS

Figure 3. Application Schematic Sheet 1/2

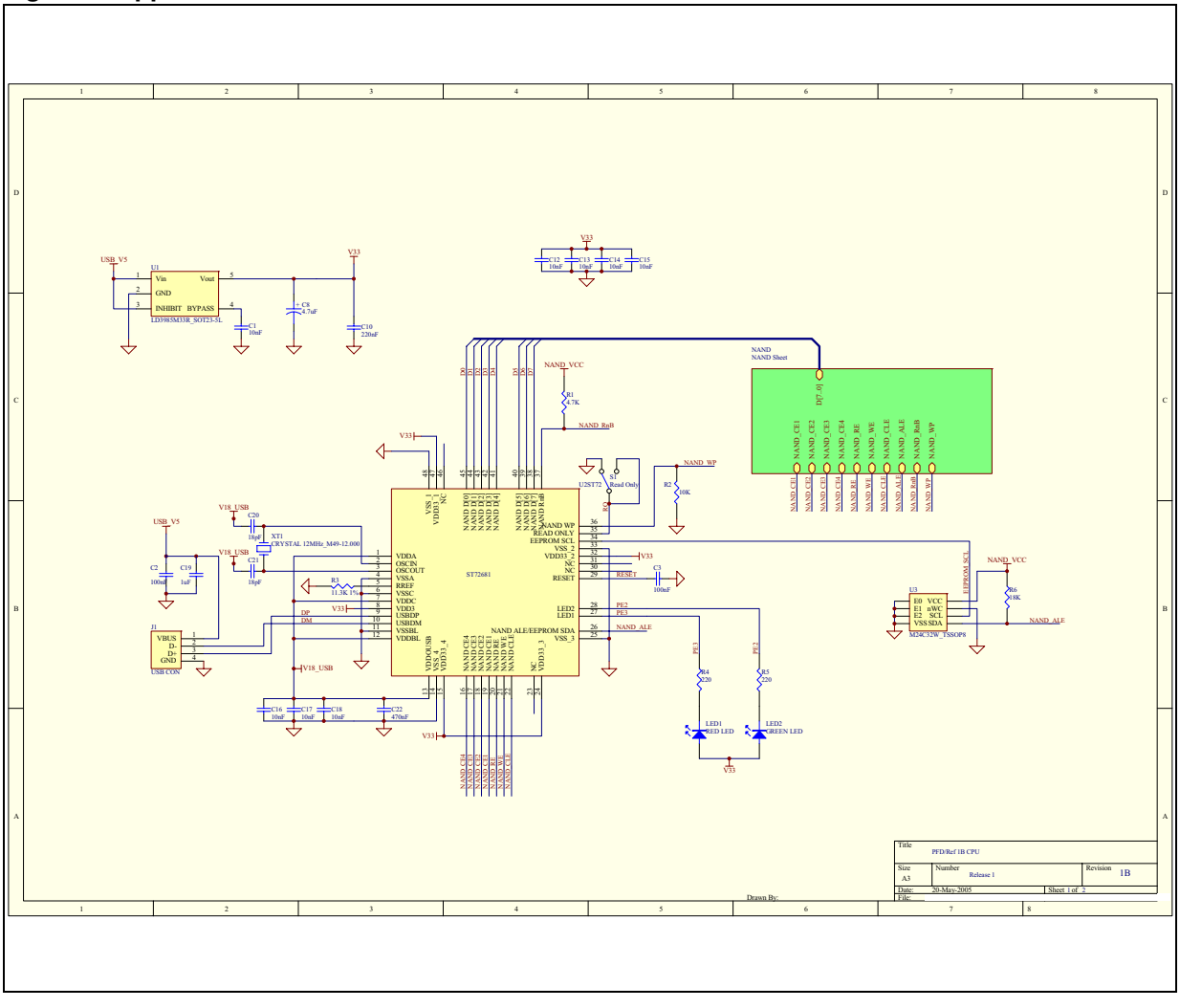
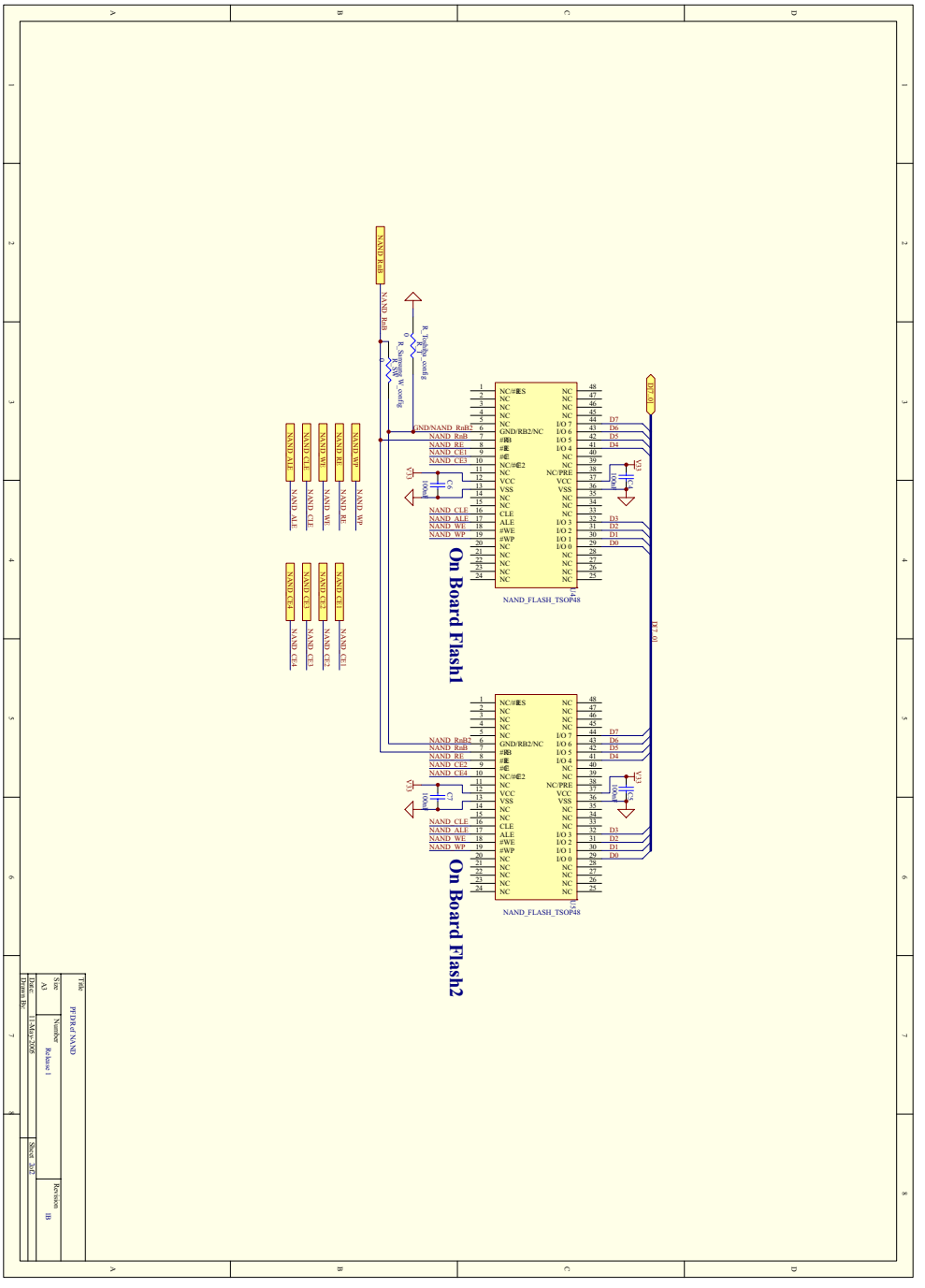
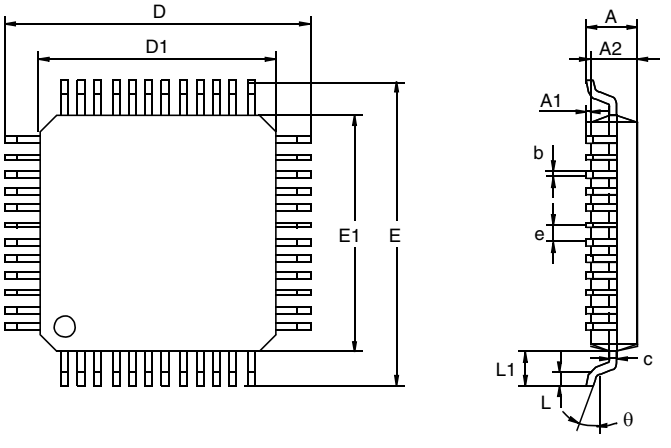


Figure 4. Application Schematic Sheet 2/2



5 PACKAGE MECHANICAL DATA

Figure 5. 48-Pin Thin Quad Flat Package



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
E		9.00			0.354	
E1		7.00			0.276	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	48					

6 REVISION HISTORY

Table 6. Revision History

Date	Revision	Description of Changes
May-2005	1.1	Changed status of the document Changed description on 1st page Removed unconnected pins in Table 5 on page 6 Changed Table 4, “USB 2.0 and core Clock System,” on page 5 Changed pin 5 description in Table 3, “USB 2.0 Interface,” on page 5 Changed section 3 on page 7 Changed Figure 3 and Figure 4

Notes: