



STP4NK50Z - STP4NK50ZFP STD4NK50Z - STD4NK50Z-1

N-CHANNEL 500V - 2.4Ω - 3A TO-220/TO-220FP/DPAK/IPAK
Zener-Protected SuperMESH™ Power MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STP4NK50Z	500 V	< 2.7 Ω	3 A	45 W
STP4NK50ZFP	500 V	< 2.7 Ω	3 A	20 W
STD4NK50Z	500 V	< 2.7 Ω	3 A	45 W
STD4NK50Z-1	500 V	< 2.7 Ω	3 A	45 W

- TYPICAL R_{DS(on)} = 2.3 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY



DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING

INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP4NK50Z	P4NK50Z	TO-220	TUBE
STP4NK50ZFP	P4NK50ZFP	TO-220FP	TUBE
STD4NK50ZT4	D4NK50Z	DPAK	TAPE & REEL
STD4NK50Z-1	D4NK50Z	IPAK	TUBE

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		STP4NK50Z	STP4NK50ZFP	STD4NK50Z STD4NK50Z-1	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	500			V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	500			V
V _{GS}	Gate- source Voltage	± 30			V
I _D	Drain Current (continuous) at T _C = 25°C	3	3 (*)	3 (*)	A
I _D	Drain Current (continuous) at T _C = 100°C	1.9	1.9 (*)	1.9 (*)	A
I _{DM} (•)	Drain Current (pulsed)	12	12 (*)	12 (*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	45	20	45	W
	Derating Factor	0.36	0.16	0.36	W/°C
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2800			V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5			V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	-	2500	-	V
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-55 to 150			°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 3 A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220	TO-220FP	DPAK IPAK	
R _{thj-case}	Thermal Resistance Junction-case (Max)	2.78	6.25	2.78	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient (Max)	62.5		100	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300			°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	3	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	120	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	I _{gs} = ± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

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ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0	500			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 50μA	3	3.75	4.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 1.5 A		2.3	2.7	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 15 V, I _D = 1.5 A		1.5		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		310 49 10		pF pF pF
C _{oss eq.} (3)	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0V to 400V		33		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	V _{DD} = 250 V, I _D = 1.5 A R _G = 4.7Ω V _{GS} = 10 V (Resistive Load see, Figure 3)		10 7		ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 400 V, I _D = 3 A, V _{GS} = 10 V		12 3 7		nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(off)} t _f	Turn-off Delay Time Fall Time	V _{DD} = 250 V, I _D = 1.5 A R _G = 4.7Ω V _{GS} = 10 V (Resistive Load see, Figure 3)		21 11		ns ns
t _{r(Voff)} t _f t _c	Off-voltage Rise Time Fall Time Cross-over Time	V _{DD} = 400V, I _D = 3 A, R _G = 4.7Ω, V _{GS} = 10V (Inductive Load see, Figure 5)		10 10 17		ns ns ns

SOURCE DRAIN DIODE

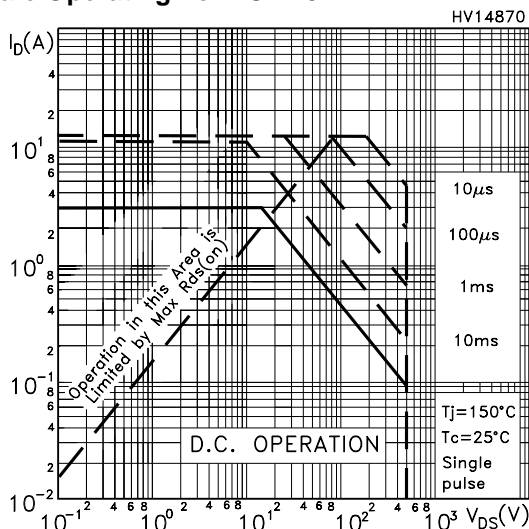
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				3 12	A A
V _{SD} (1)	Forward On Voltage	I _{SD} = 3 A, V _{GS} = 0			1.6	V
t _{rr} Q _{rr} I _R RRM	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 3 A, di/dt = 100A/μs V _{DD} = 40 V, T _j = 150°C (see test circuit, Figure 5)		260 935 7.2		ns nC A

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

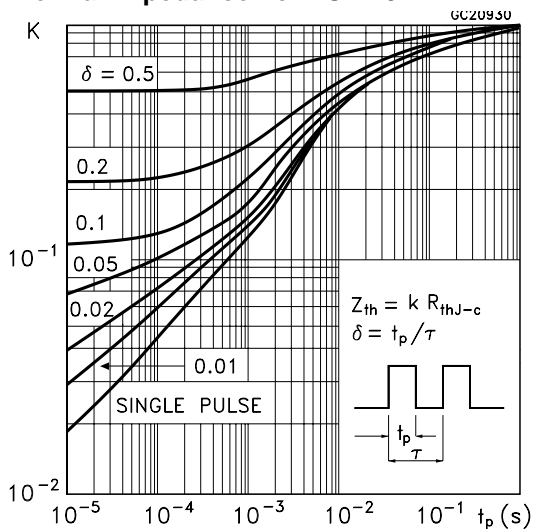
2. Pulse width limited by safe operating area.

3. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

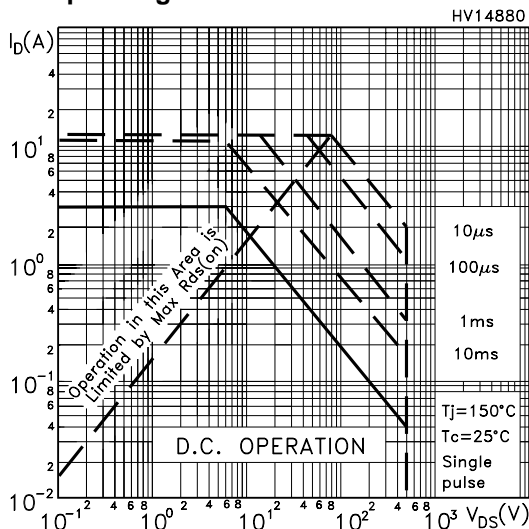
Safe Operating For TO-220



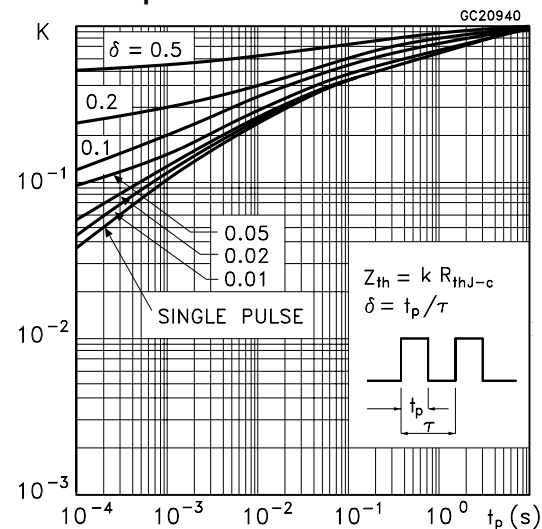
Thermal Impedance For TO-220



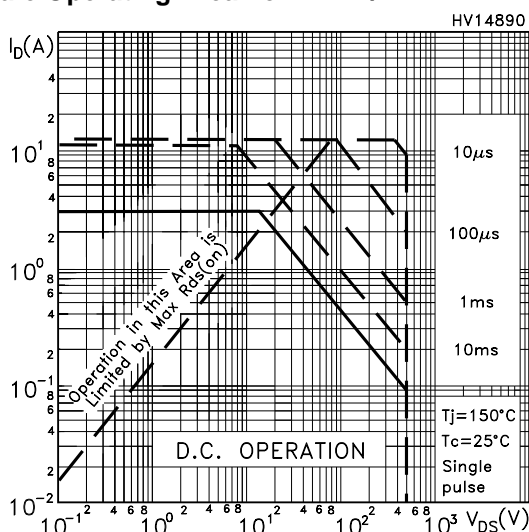
Safe Operating Area For TO-220FP



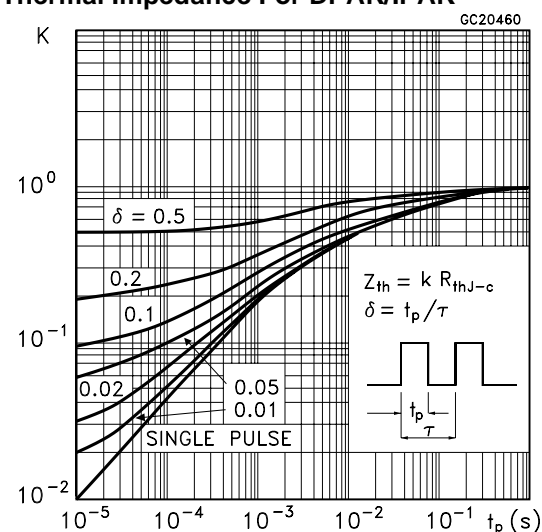
Thermal Impedance For TO-220FP



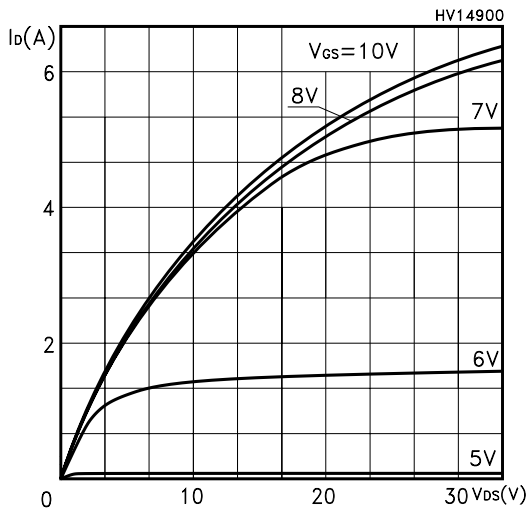
Safe Operating Area For DPAK/IPAK



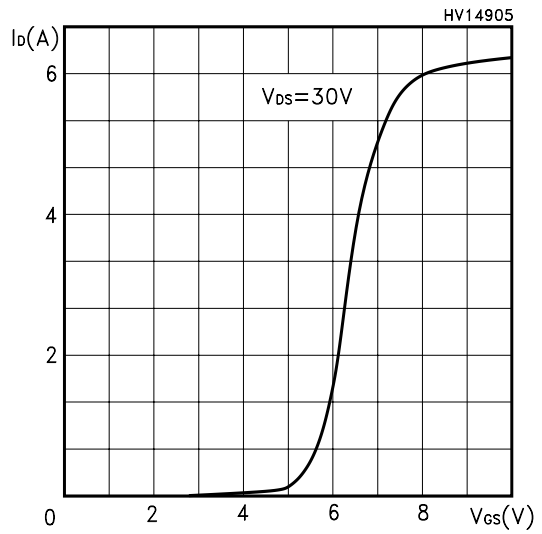
Thermal Impedance For DPAK/IPAK



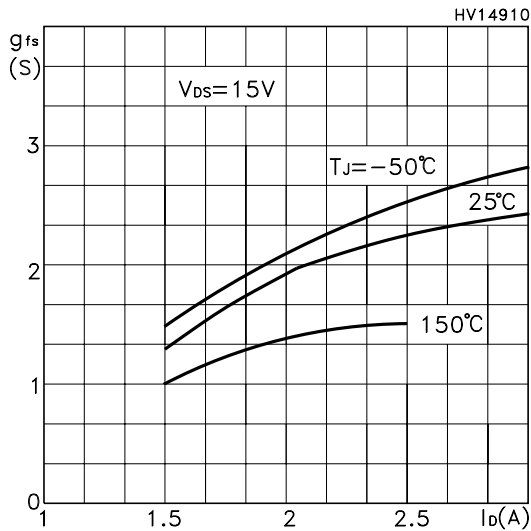
Output Characteristics



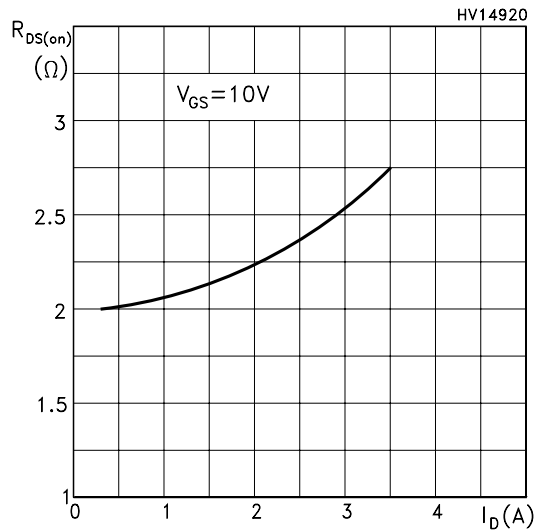
Transfer Characteristics



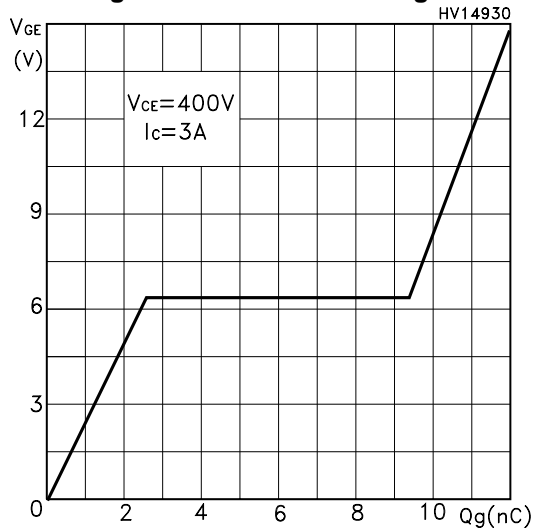
Transconductance



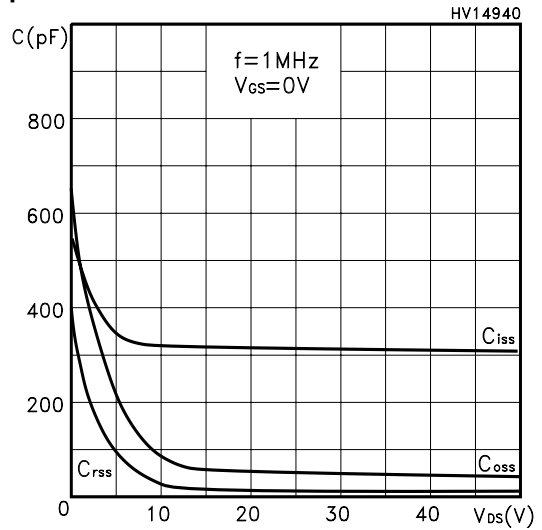
Static Drain-source On Resistance



Gate Charge vs Gate-source Voltage

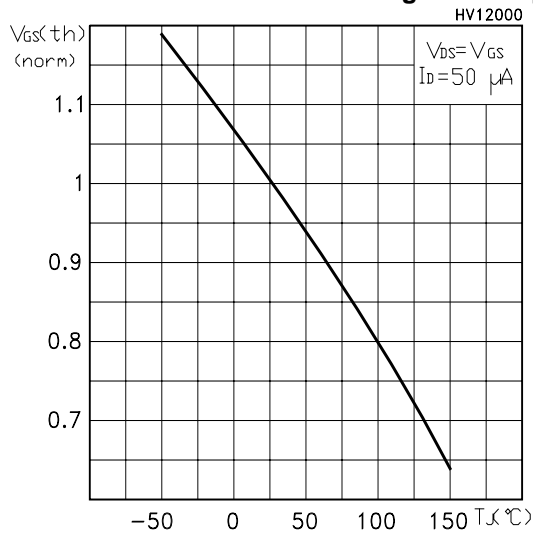


Capacitance Variations

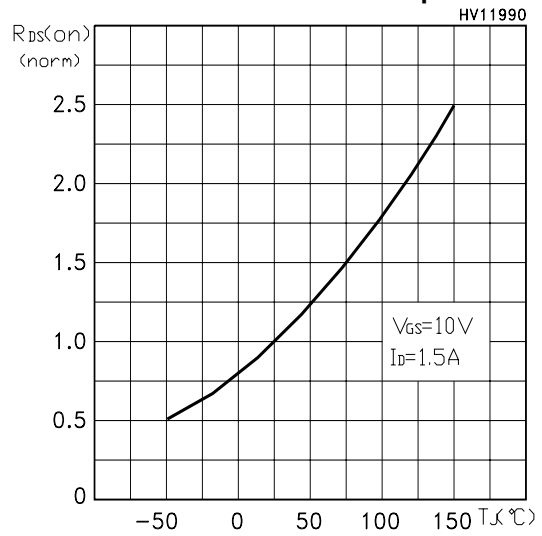


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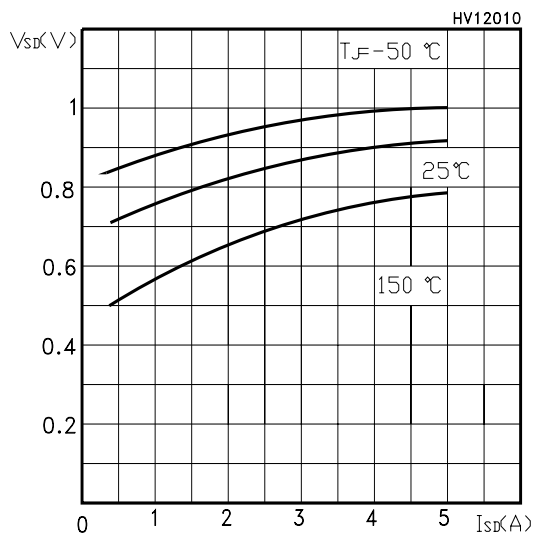
Normalized Gate Threshold Voltage vs Temp.



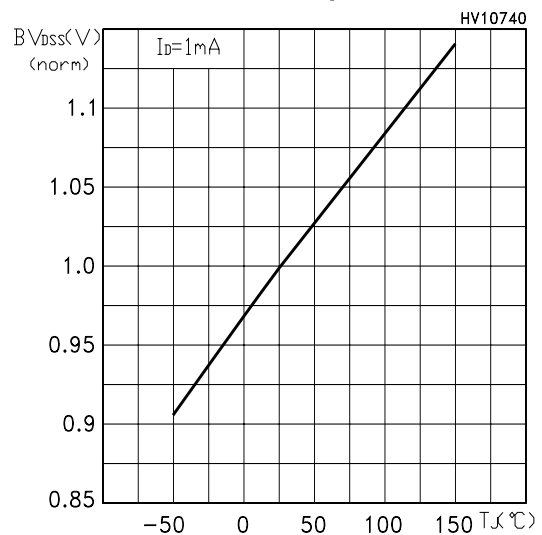
Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized BVDSS vs Temperature



Maximum Avalanche Energy vs Temperature

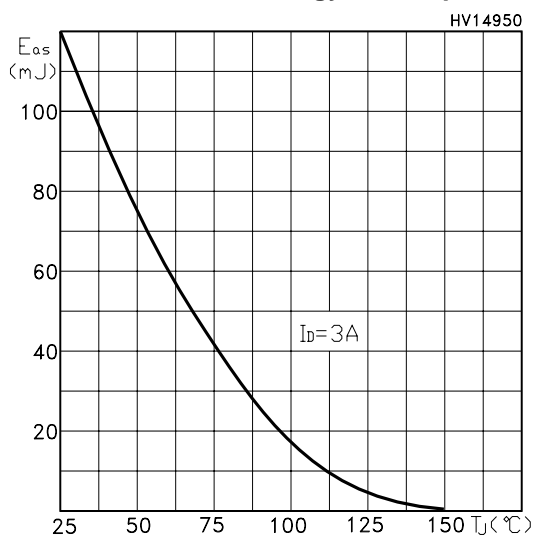


Fig. 1: Unclamped Inductive Load Test Circuit



Fig. 2: Unclamped Inductive Waveform



Fig. 3: Switching Times Test Circuit For Resistive Load



Fig. 4: Gate Charge test Circuit



Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



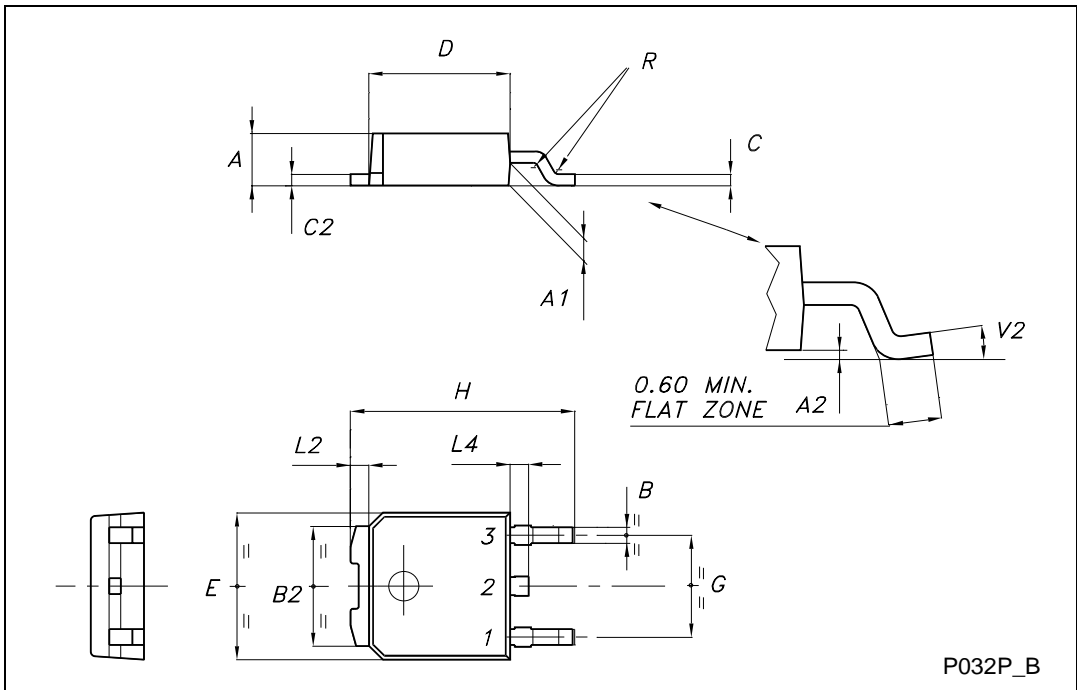
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.5	0.045		0.067
F2	1.15		1.5	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



P032P_B

TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



DPAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

TOP COVER TAPE

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

FEED DIRECTION

Bending radius R min.

* on sales type



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