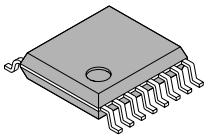
MB15ExxSL Series

Single PLL Frequency Synthesizers with On-Chip Prescalers

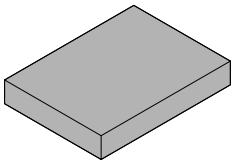
Description

The Fujitsu ExxSL series single PLLs are serial input frequency synthesizers operating up to 2.5 GHz. They have built-in dual-modulus prescalers enabling pulse swallow operation. The latest advanced BiCMOS technology is used resulting in a super low supply current. A refined charge pump design (Fujitsu's Super Charger) provides fast tuning along with low spurious noise and phase noise characteristics. The E-series is ideally suited for digital mobile communications, including GSM, DCS1800, PCS1900, IS-136, IS-95 and ISM applications.

Packages



16-pin plastic SSOP, FPT-16P-M05



16-pin plastic BCC, LCC-16P-M06

Features

- Very low spurious and phase noise characteristics
- Excellent lock-up time performance
- Low operating voltage: 2.4 to 3.6 volts
- Super low operating current: 2.5 to 4.0 mA (typical)
- Power-saving current: 0.1µA (typical)
- Selectable charge pump current (±1.5 or ±6.0 mA)
- Wide operating temperature: –40 to +85°C
- Plastic 16-pin SSOP and 16-pin BCC packages
- Reference counter:
  - 14-bit programmable divider: 3 to 16383
- 18-bit programmable divider:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 3 to 2047
- Evaluation kits available

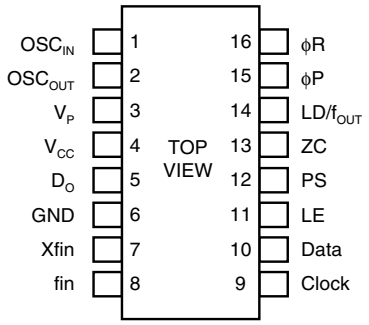
Parameter	MB15E03SL	MB15E05SL	MB15E07SL
RF Frequency of Operation	1.2 GHz	2.0 GHz	2.5 GHz
Low Power Supply Voltage	2.7V	2.7V	2.7V
Low Power Supply Current	2.0 mA	3.0 mA	3.5 mA
Prescaler Divide Ratios	64/65 or 128/129		32/33 or 64/65
Power-Saving Function	0.1µA typ.		

Table of Contents

Pin Descriptions

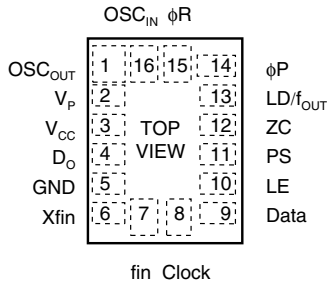
Pin No.		Pin Name	I/O	Descriptions
SSOP	BCC			
1	16	OSC_{IN}	I	Programmable reference divider input Oscillator input connection to a TCXO
2	1	OSC_{OUT}	O	Oscillator output
3	2	V_P	—	Power supply voltage input for the charge pump
4	3	V_{CC}	—	Power supply voltage input
5	4	Do	O	Charge pump output Phase of the charge pump can be selected via programming of the FC bit.
6	5	GND	—	Ground
7	6	Xfin	I	Prescaler complementary input which should be grounded via a capacitor.
8	7	fin	I	Prescaler input Connection to an external VCO should be done via AC coupling.
9	8	Clock	I	Clock input for 19-bit shift register Data is shifted into shift register on rising edge of the clock. (Open is prohibited.)
10	9	Data	I	Serial data input using binary code Last bit of data is a control bit. (Open is prohibited.)
11	10	LE	I	Load enable signal input. (Open is prohibited.) When LE is set high, data in the shift register is transferred to a latch according to control bit in the serial data.
12	11	PS	I	Power-saving mode control. Pin must be set at "L" at Power-ON. (Open is prohibited.) PS = "H" sets normal mode. PS = "L" sets power-saving mode.
13	12	ZC	I	Forced high-impedance control for the charge pump (with internal pull up resistor) ZC = "H" sets normal Do output. ZC = "L"; Do becomes high impedance.
14	13	LD/f_{OUT}	O	Lock detect signal output (LD)/phase comparator monitoring output (f_{OUT}) The output signal is selected via programming of the LDS bit. LDS = "H" outputs f_{OUT} (fr/fp monitoring output). LDS = "L" outputs LD ("H" = locked state, "L" = unlocked state).
15	14	ϕP	O	Phase comparator N-channel open drain output for an external charge pump. Phase can be selected via programming of the FC bit.
16	15	ϕR	O	Phase comparator CMOS output for an external charge pump. Phase can be selected via programming of the FC bit.

16-pin SSOP



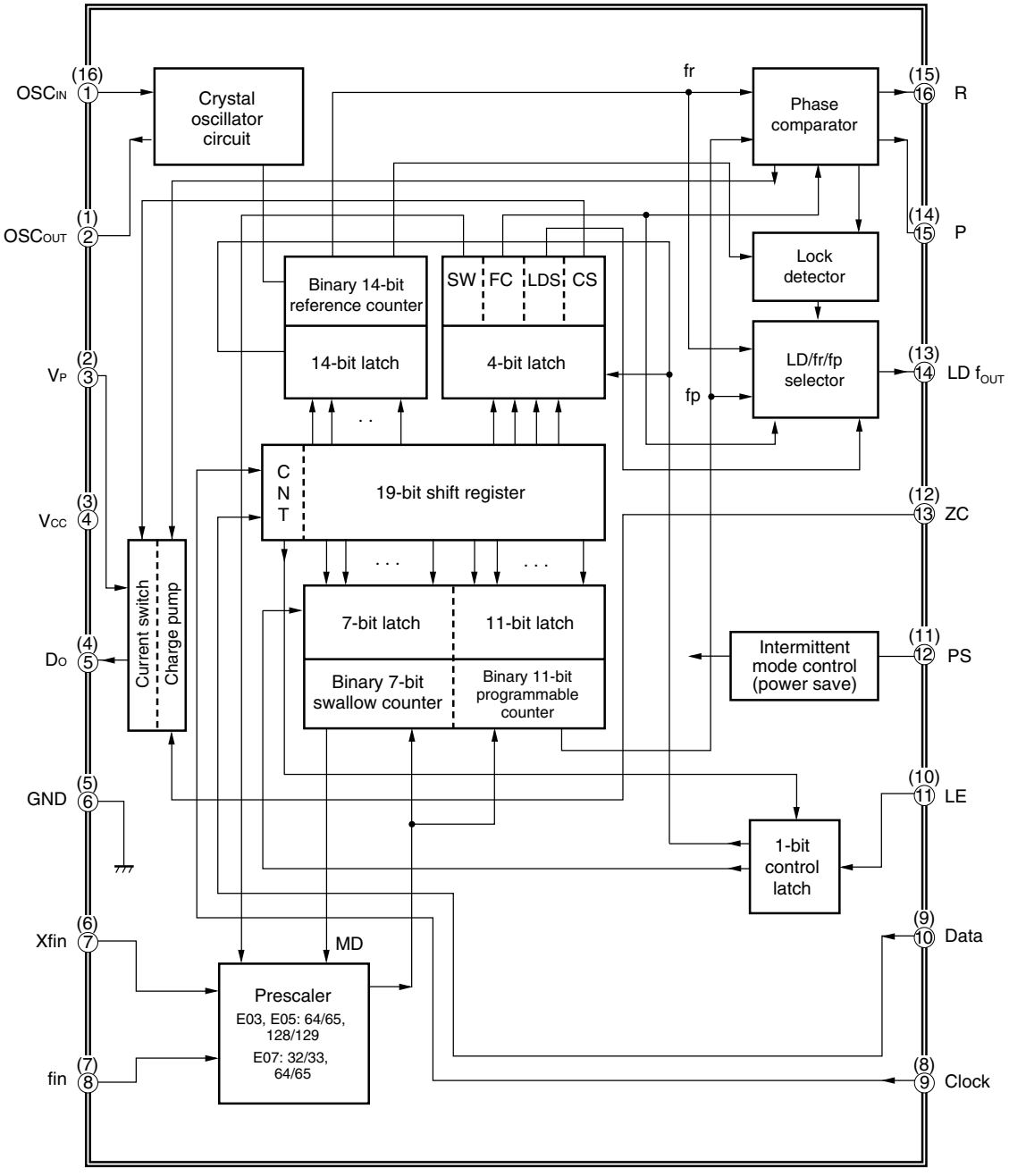
FPT-16P-M05

16-pad BCC



LCC-16P-M06

Block Diagram



○ : SSOP
( ) : BCC

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remark
			Min.	Max.		
Power supply voltage	V_{CC}	–	–0.5	4.0	V	
	V_P	–	V_{CC}	6.0	V	
Input voltage	V_I	–	–0.5	V_{CC} +0.5	V	
Output voltage	V_O	Except Do	GND	V_{CC}	V	
	V_O	Do	GND	V_P	V	
Storage temperature	Tstg	–	–55	+125	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.4	3.0	3.6	V	
	V_P	V_{CC}	–	5.5	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges. Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Fujitsu representative beforehand.

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

Electrical Characteristics

Device Specifications

V_{CC} = 2.4 to 3.6 V, Ta = –40 to +85°C

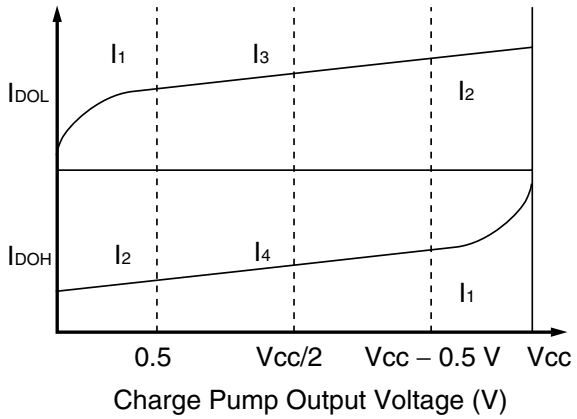
Parameter	Symbol	MB15E03SL	MB15E05SL	MB15E07SL
Power supply current	I_{CCRF}*1	2.0 mA	3.0 mA	3.5 mA
Power-saving current	I_{PSRF}*2	0.1µA	0.1µA	0.1µA
Operating frequency	fin_{RF}	0.1 - 1.2 GHz	0.1 - 2.0 GHz	0.1 - 2.5 GHz
	OSC_{in}*3	3 - 40 MHz	3 - 40 MHz	3 - 40 MHz

General Specifications

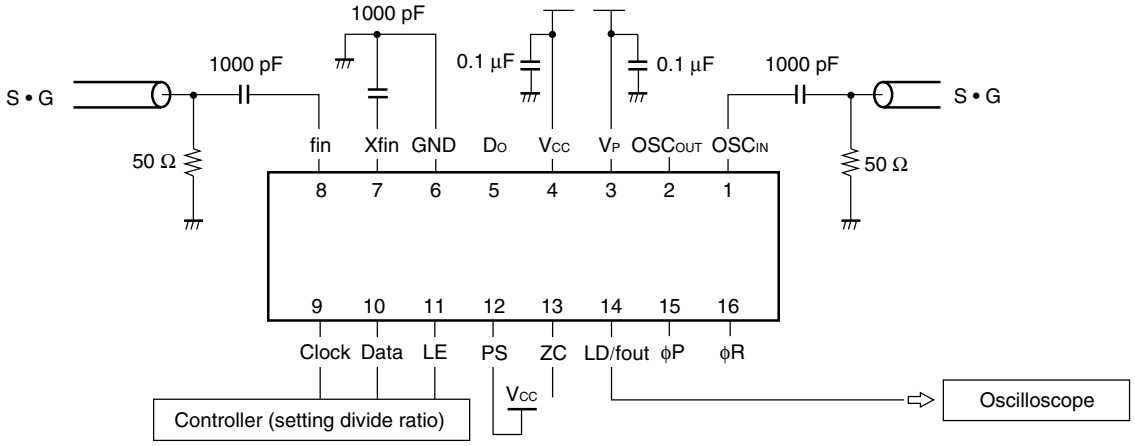
Parameter		Symbol	Condition		Value Min.	Value Typ.	Value Max.	Unit
Input sensitivity	fin_{RF}	$Pfin_{RF}$	50Ω load system (Refer to measurement circuit.)		–15	–	+2	dBm
	OSC_{IN}	V_{OSC}	–		0.5	–	V_{CC}	Vp-p
Input voltage	Data, Clock, LE, PS, ZC	V_{IH}	–		$V_{CC} \times 0.7$	–	–	V
		V_{IL}	–		–	–	$V_{CC} \times 0.3$	
Input current	Data, Clock, LE, PS	I_{IH}*4	–		–1.0	–	1.0	µA
		I_{IL}*4	–		–1.0	–	1.0	
	OSC_{IN}	I_{IH}	–		0	–	100	µA
		I_{IL}*4	–		–100	–	0	
	ZC	I_{IH}	–		–1.0	–	1.0	µA
		I_{IL}*4	Pull up input		–100	–	0	
Output voltage	ϕP	V_{OL}	Open drain output		–	–	0.4	V
	ϕR, LD/f_{OUT}	V_{OH}	$V_{CC} = V_P$ = 3.0V, I_{OH} = –1 mA		V_{CC} –0.4	–	–	V
		V_{OL}	$V_{CC} = V_P$ = 3.0V, I_{OL} = 1 mA		–	–	0.4	
	Do	V_{DOH}	$V_{CC} = V_P$ = 3.0V, I_{OH} = –0.5 mA		V_{CC} –0.4	–	–	V
		V_{DOL}	$V_{CC} = V_P$ = 3.0V, I_{OL} = 0.5 mA		–	–	0.4	
High impedance cutoff current	Do	I_{OFF}	$V_{CC} = V_P$ = 3.0V V_{OFF} = .5V to V_P-0.5V		–	–	2.5	nA
Output current	ϕP	I_{OL}	Open drain output		1.0	–	–1.0	mA
	ϕR, LD/f_{OUT}	I_{OH}*4	V_{CC} = 3.0V		–	–	–	mA
		I_{OL}	V_{CC} = 3.0V		1.0	–	–	mA
	Do	I_{DOH}*4	$V_{CC} = V_P$ = 3.0 , $V_{DOH} = V_P/2$, Ta = +25°C	CS bit = "H"	–	–6.0	–	mA
				CS bit = "L"	–	–1.5	–	mA
		I_{DOL}	$V_{CC} = V_P$ = 3.0V, $V_{DOL} = V_P/2$, Ta = +25°C	CS bit = "H"	–	6.0	–	mA
				CS bit = "L"	–	1.5	–	mA
Charge pump current characteristics	I_{DOL}/I_{DOH}	I_{DOMT}*5	$V_{DO} = V_{CC}/2$		–	3	–	%
	vs V_{DO}	I_{DOVD}*6	0.5V ≤ V_{DO} ≤ V_{CC} – 0.5V		–	10	–	%
	vs Ta	I_{DOTA}*7	–40°C ≤ Ta ≤ +85°C, $V_{DO} = V_{CC}/2$		–	10	–	%

Note: See footnotes on next page.

*1 Conditions: fosc = 12 MHz, Ta = +25°C in locking state, V_{CC} = 2.7 V
*2 V_{CCIF} = V_{CCRF} = 3.0 V, fosc = 12.8 MHz, Zc = "H" or open, Ta = +25°C in power-saving mode
*3 AC coupling. 1000pF capacitor is connected under the condition of minimum operating frequency.
*4 The symbol "–" (minus) means direction of current flow.
*5 V_{CC} = 3.0 V, Ta = +25°C $(|I_3| - |I_4|)/[(|I_3| + |I_4|)/2] \times 100(\%)$
*6 V_{CC} = 3.0 V, Ta = +25°C $[(|I_2| - |I_1|)/2]/[(|I_1| + |I_2|)/2] \times 100(\%)$ (Applied to each I_{DOL}, I_{DOH})
*7 V_{CC} = 3.0 V, $[|I_{DO(85°C)} - I_{DO(-40°C)}|/2]/[|I_{DO(85°C)} + I_{DO(-40°C)}|/2] \times 100(\%)$ (applied to each I_{DOL}, I_{DOH})



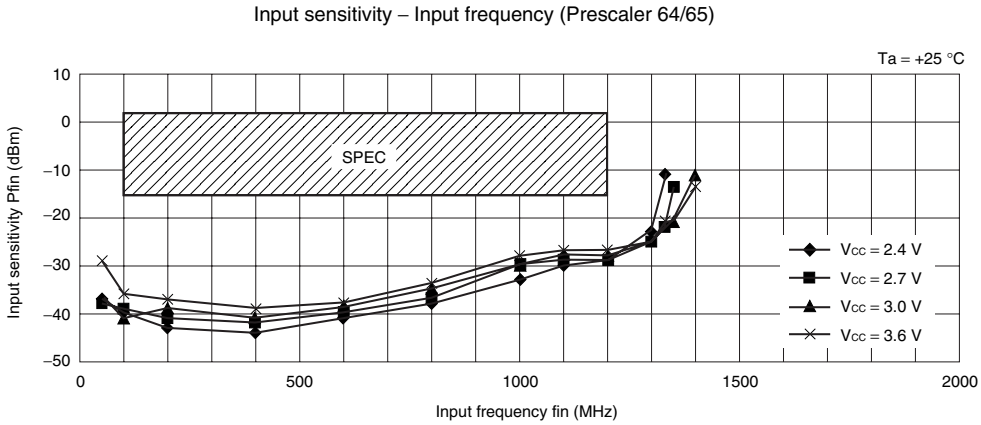
Measurement Circuit (For Measuring Input Sensitivity of fin and OSC_{IN})



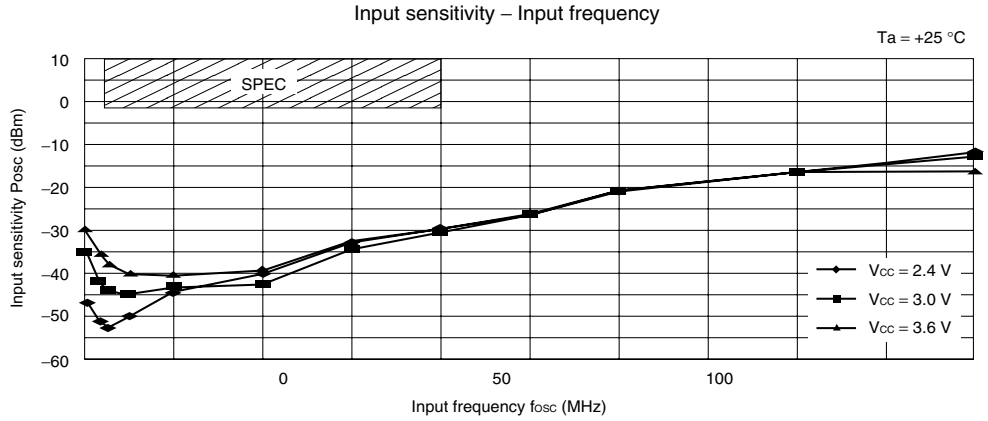
Note: 16-pin SSOP

Typical Electrical Characteristics: MB15E03SL

Input Sensivity of f_{IN} Versus Input Frequency



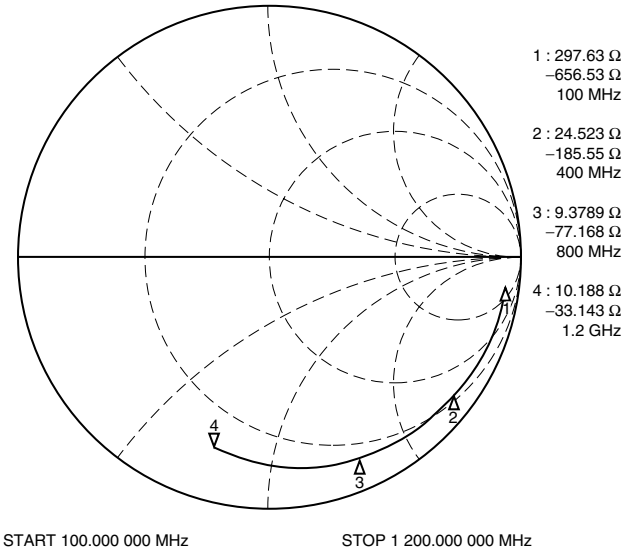
Input Sensivity of OSC_{IN} versus Input Frequency



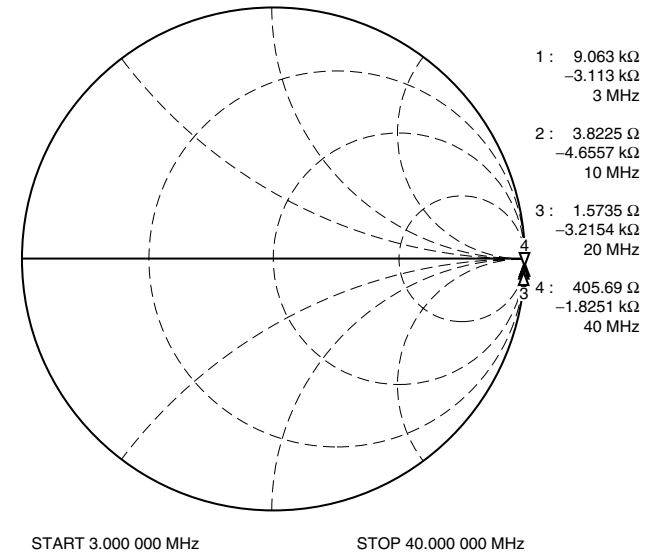
Typical Electrical Characteristics: MB15E03SL

Input Impedance

fin Pin

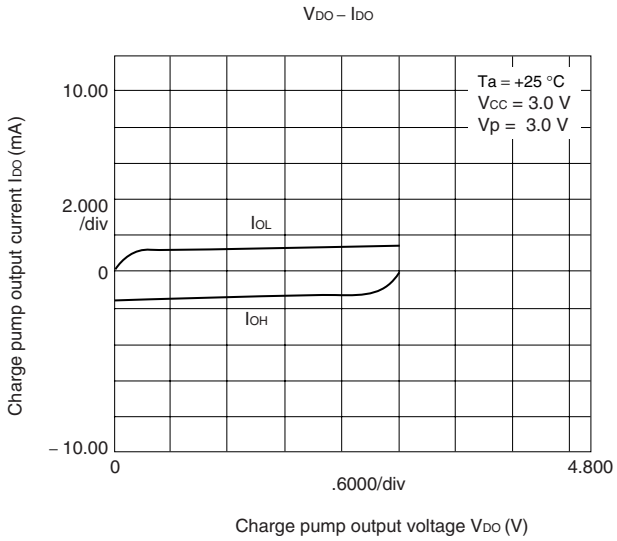


OSC_{IN} Pin

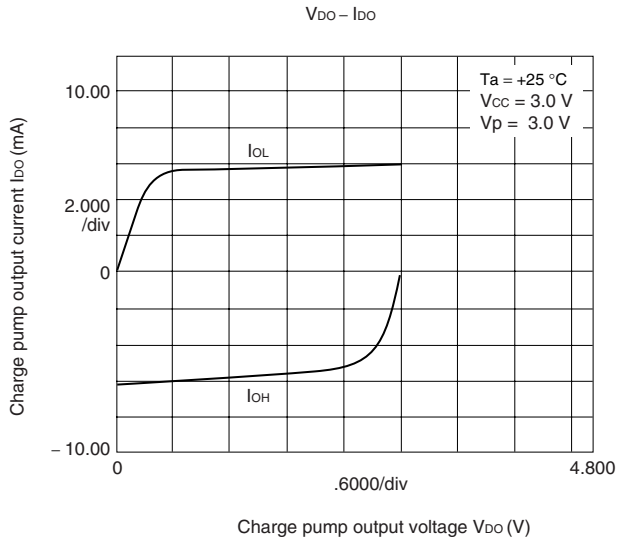


Typical Electrical Characteristics: MB15E03SL

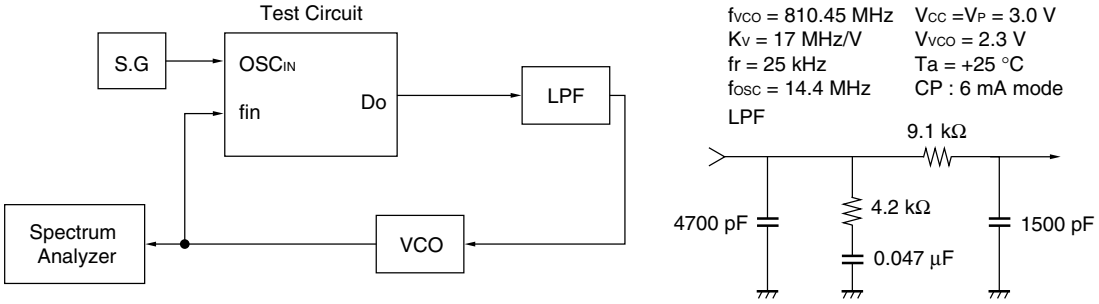
Do ouput current: 1.5 mA mode



Do ouput current: 6.0 mA mode

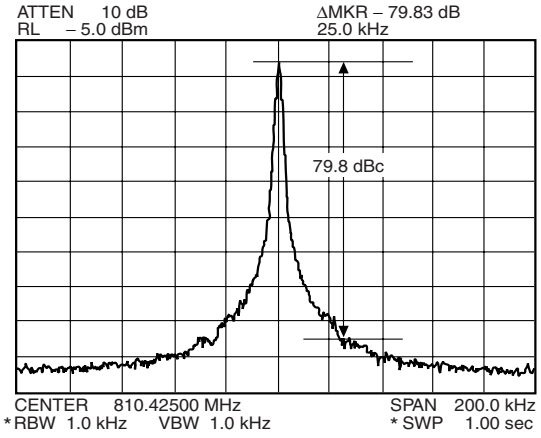


Reference Information: MB15E03SL

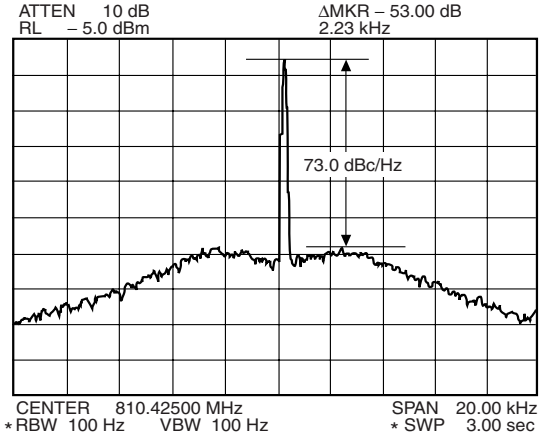


Typical plots measured with the test circuit are shown below. The plots show lock up time, phase noise and reference leakage.

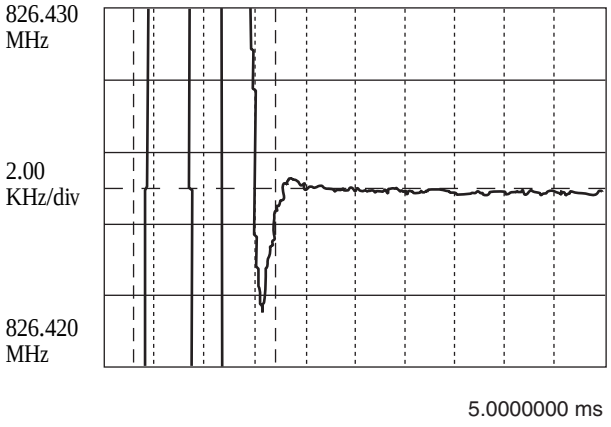
PLL Reference Leakage
@ 25 kHz offset = -79.8 dBc



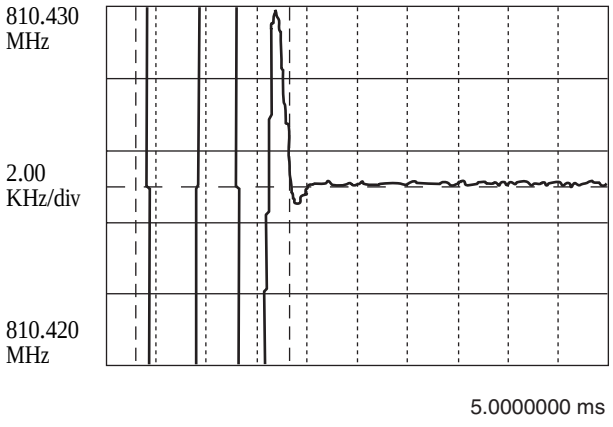
PLL Phase Noise
@ max within loop band = -73.0 dBc/Hz



PLL Lock Up Time = 1.4 ms
(810.425 MHz → 826.425 MHz, within ± 1kHz)

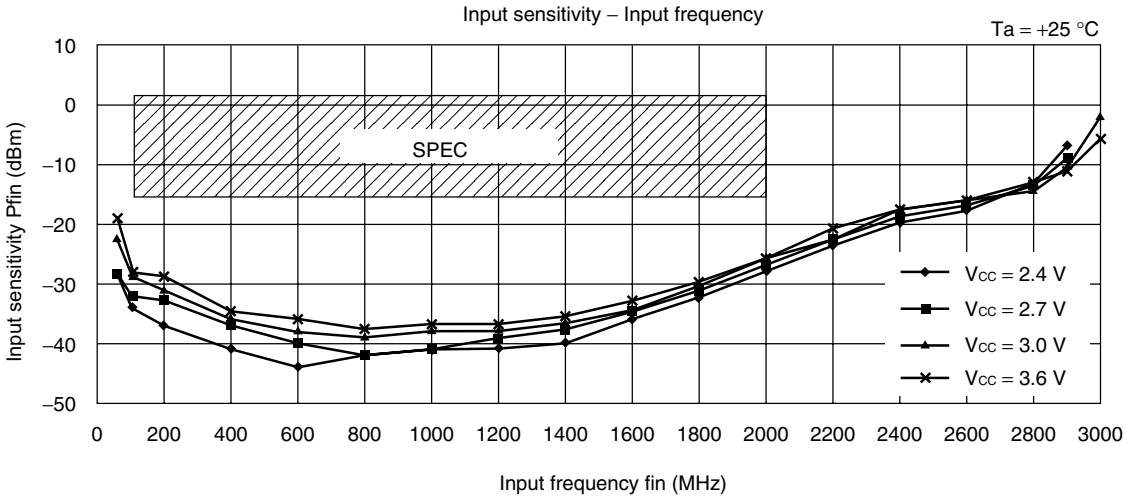


PLL Lock Up Time = 1.52 ms
(826.425 MHz → 810.425 MHz, within ± 1kHz)

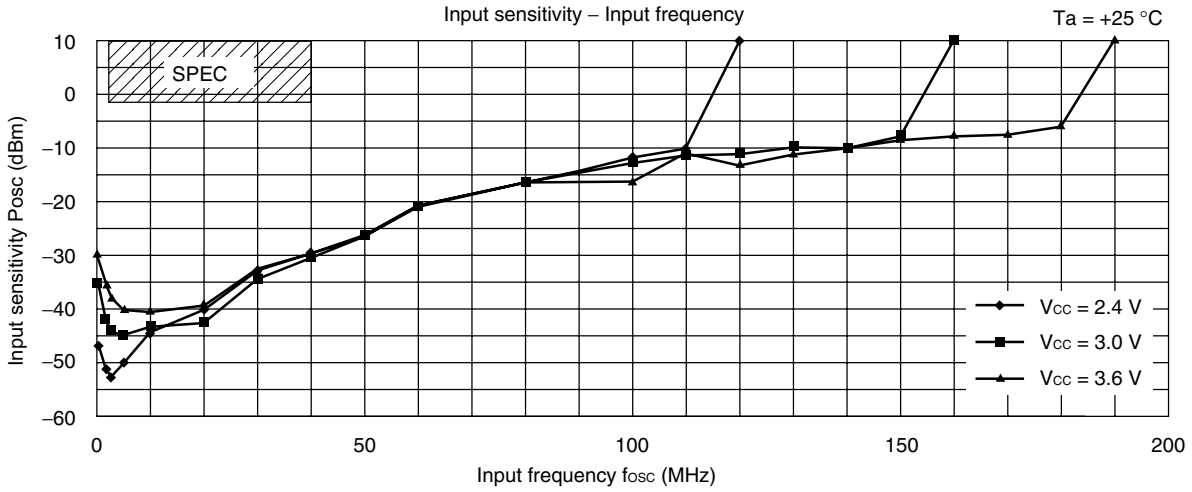


Typical Electrical Characteristics: MB15E05SL

Input Sensivity of f_{IN} Versus Input Frequency



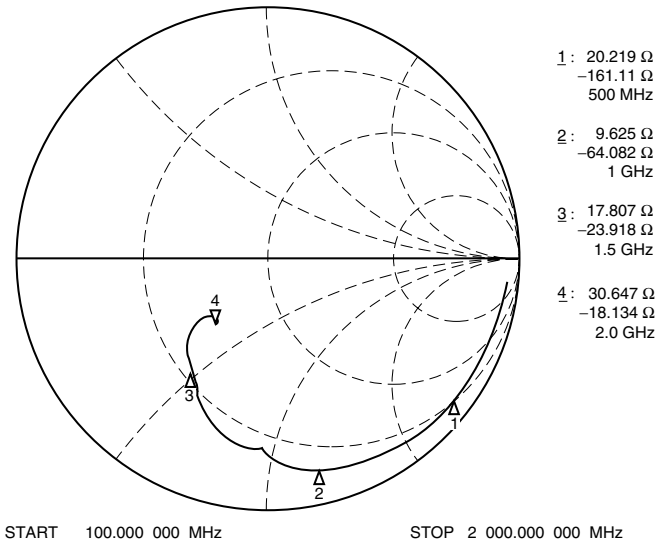
Input Sensivity of OSC_{IN} Versus Input Frequency



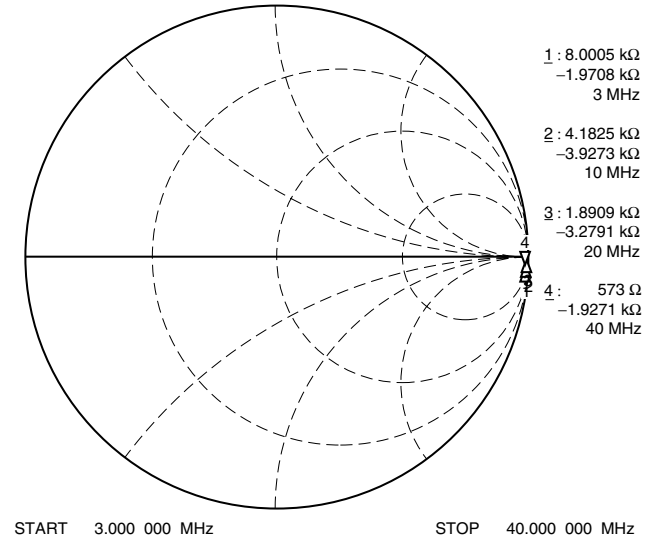
Typical Electrical Characteristics: MB15E05SL

Input Impedance

fin Pin

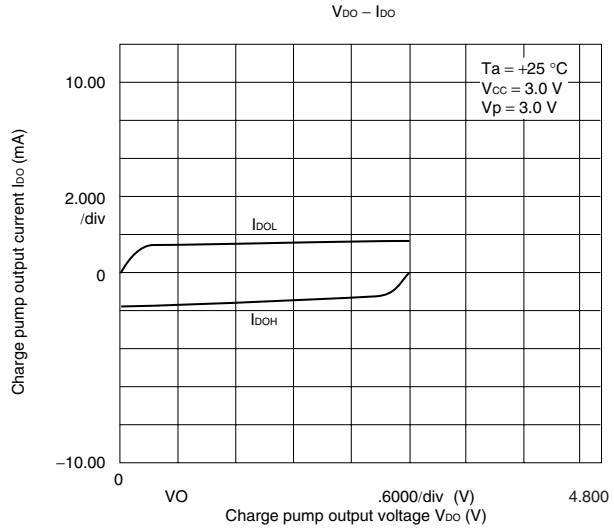


OSC_{IN} Pin

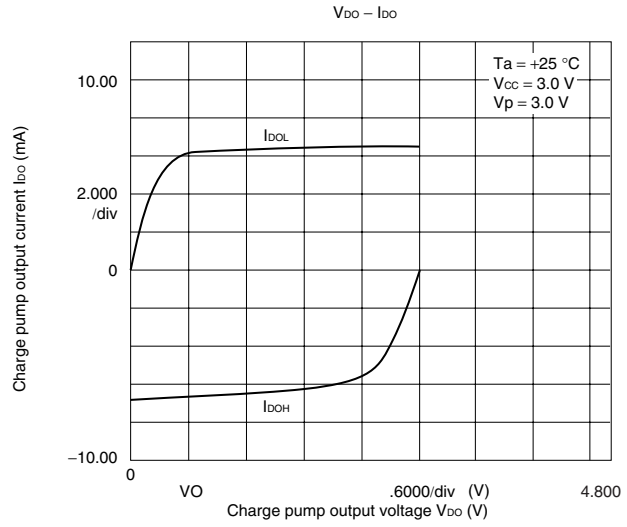


Typical Electrical Characteristics: MB15E05SL

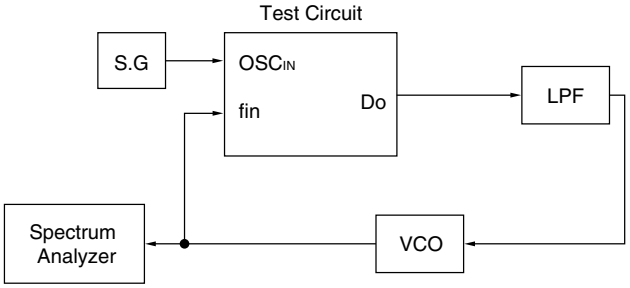
Do ouput current: 1.5 mA mode



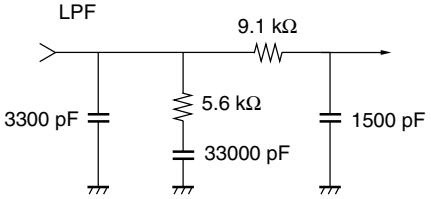
Do ouput current: 6.0 mA mode



Reference Information: MB15E05SL

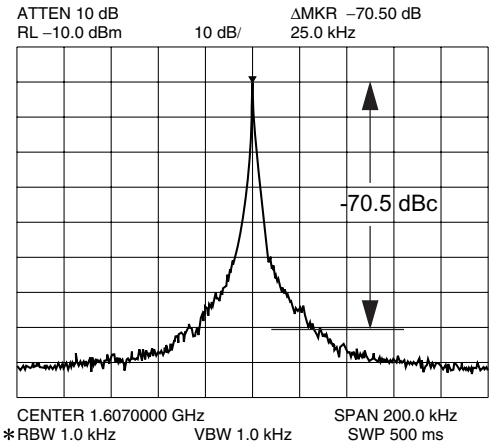


f_{VCO} = 1607 MHz
K_V = 28 MHz/V
fr = 25 kHz
f_{OSC} = 14.4 MHz
V_{CC} = V_P = 3.0 V
V_{VCO} = 2.1 V
Ta = +25 °C
CP : 6 mA mode

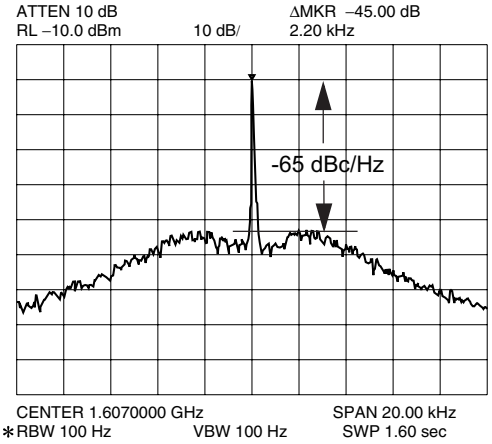


Typical plots measured with the test circuit are shown below. The plots show lock up time, phase noise and reference leakage.

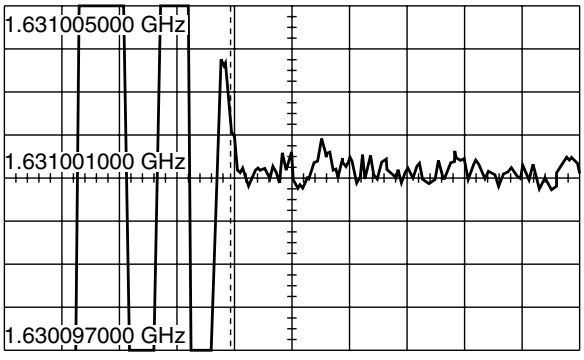
RF PLL Reference Leakage
@ 25 kHz offset = -70.5 dBc



RF PLL Phase Noise
@ max within loop band = -65 dBc/Hz

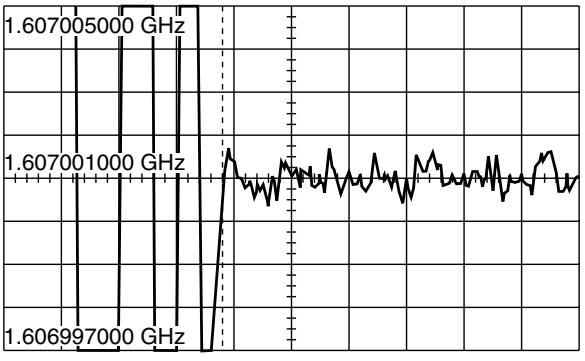


RF PLL Lock Up Time = 1.46 ms
(1607.000 MHz → 1631.000 MHz, within ± 1kHz)



500.0 µs/div

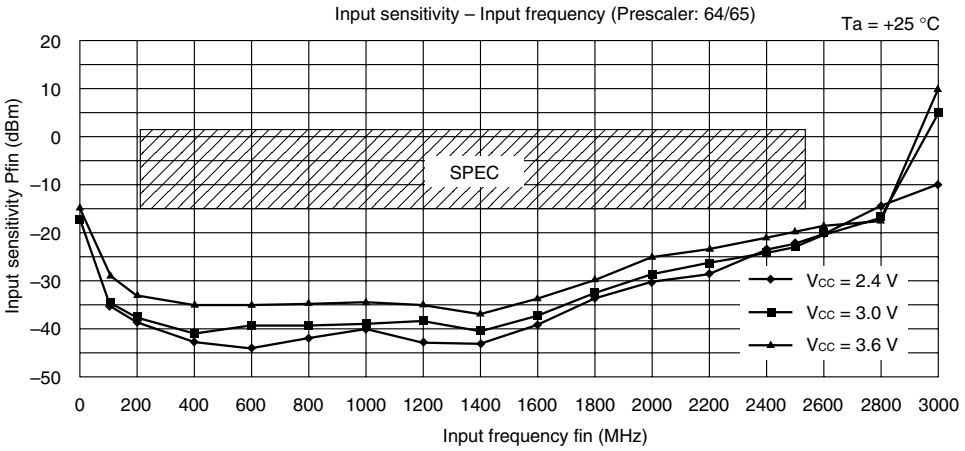
RF PLL Lock Up Time = 1.37 ms
(1631.000 MHz → 1607.000 MHz, within ± 1kHz)



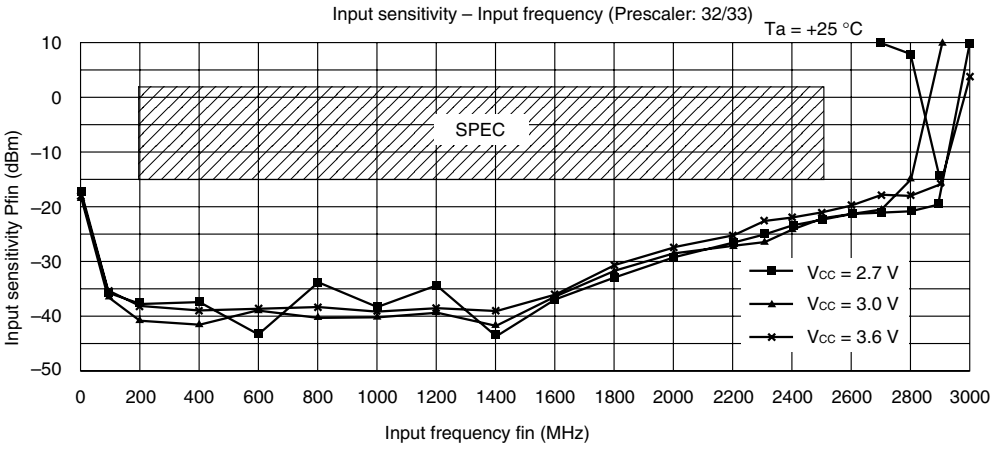
500.0 µs/div

Typical Electrical Characteristics: MB15E07SL

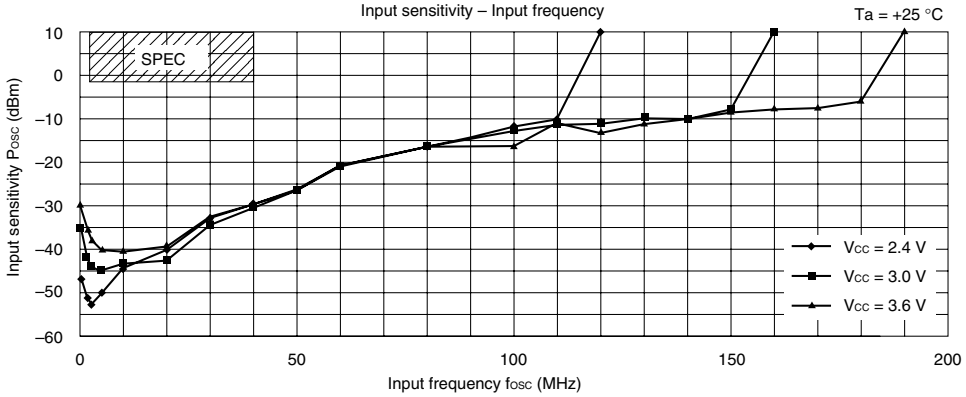
Input Sensivity of f_{IN} Versus Input Frequency



Input Sensivity of f_{IN} Versus Input Frequency



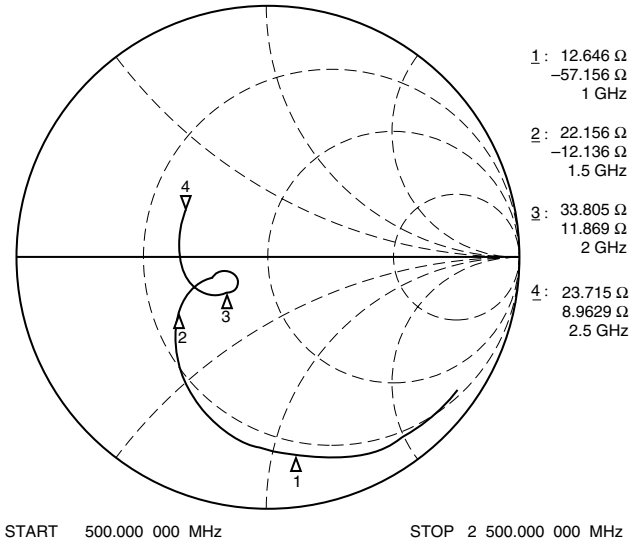
Input Sensivity of OSC_{IN} Versus Input Frequency



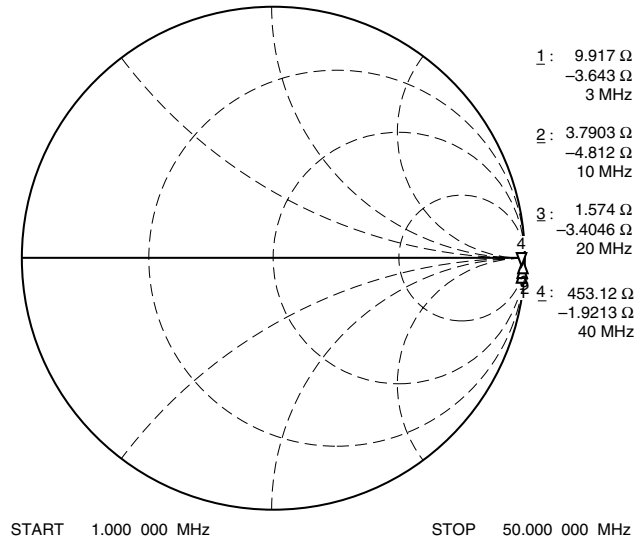
Typical Electrical Characteristics: MB15E07SL

Input Impedance

fin Pin

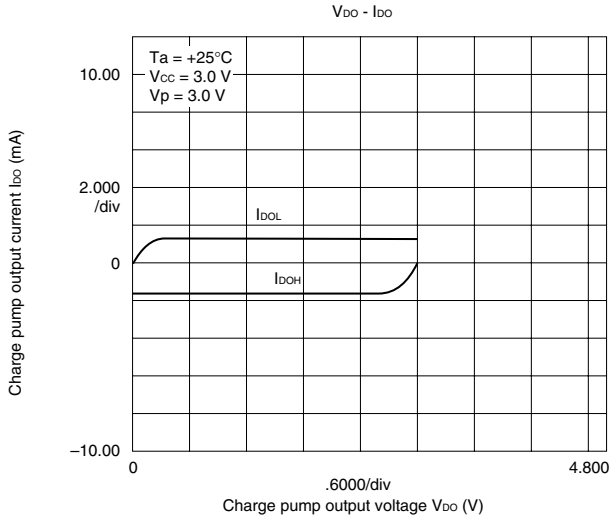


OSC_{IN} Pin

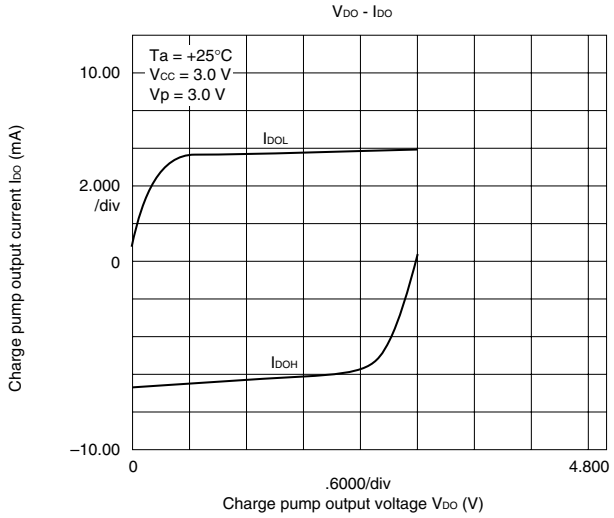


Typical Electrical Characteristics: MB15E07SL

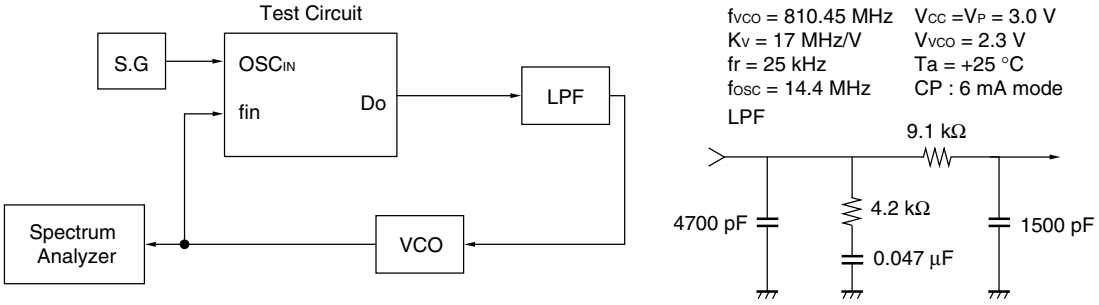
Do ouput current: 1.5 mA mode



Do ouput current: 6.0 mA mode



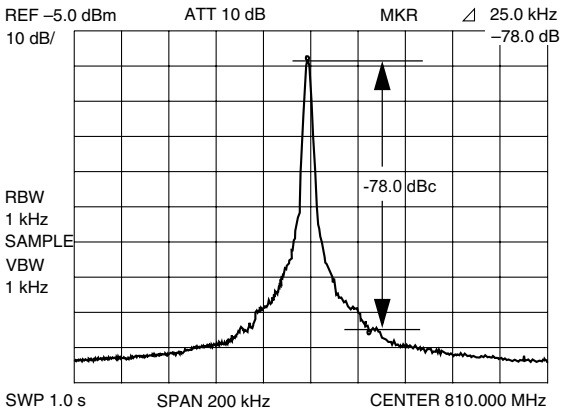
Reference Information: MB15E07SL



Typical plots measured with the test circuit are shown below. The plots show lock up time, phase noise and reference leakage.

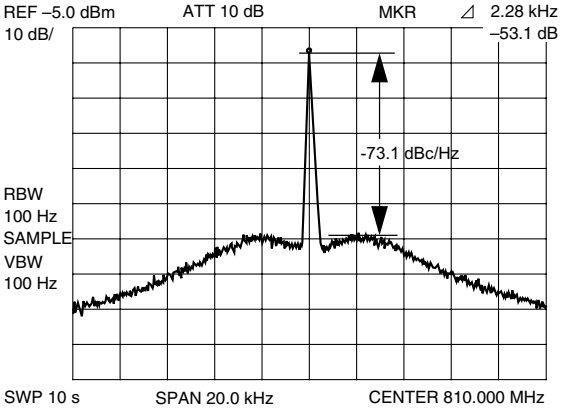
PLL Reference Leakage

@ 25 kHz offset = -78 dBc



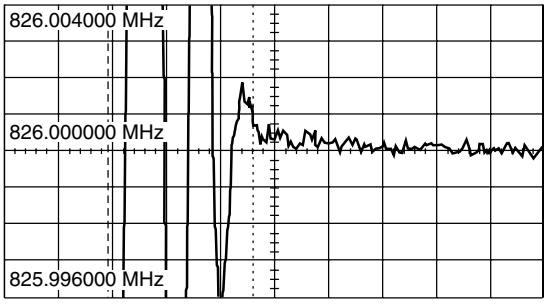
PLL Phase Noise

@ max within loop band = -73.1 dBc/Hz



PLL Lock Up Time = 1.3 ms

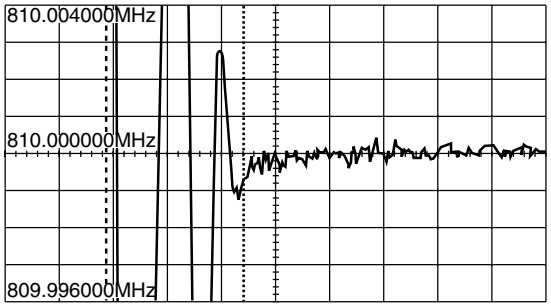
(810.000 MHz → 826.000 MHz, within ± 1kHz)



500.0 µs/div

PLL Lock Up Time = 1.28 ms

(826.000 MHz → 810.000 MHz, within ± 1kHz)



500.0 µs/div

Functional Descriptions

The VCO output frequency can be calculated using the following equation:

$f_{VCO} = \{(M \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

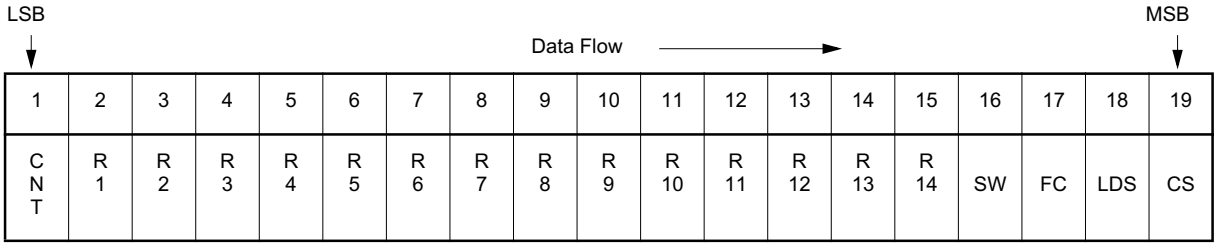
f_{VCO} Output frequency of external voltage controlled ocillator (VCO)
M Preset divide ratio of dual modulus prescaler (64 or 128 for MB15E03SL, MB15E05SL) (32 or 64 for MB15E07SL)
N Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
f_{OSC} Reference oscillation frequency
R Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

Table 1. Control Bits

Control Bit (CNT)	Destination of Serial Data
H	Programmable reference counter latch
L	Programmable counter latch

Shift Register Configuration

Programmable Reference Counter



CNT	Control bit	[Table 1]
R1 to R14	Divide ratio setting bits for the programmable reference counter (3 to 16,383)	[Table 2]
SW	Divide ratio setting bit for the prescaler	[Table 5]
FC	Phase control bit for the phase comparator	[Table 6]
LDS	LD/f_{OUT} signal select bit	[Table 7]
CS	Charge pump current select bit	[Table 8]

Note: Input data with MSB first.

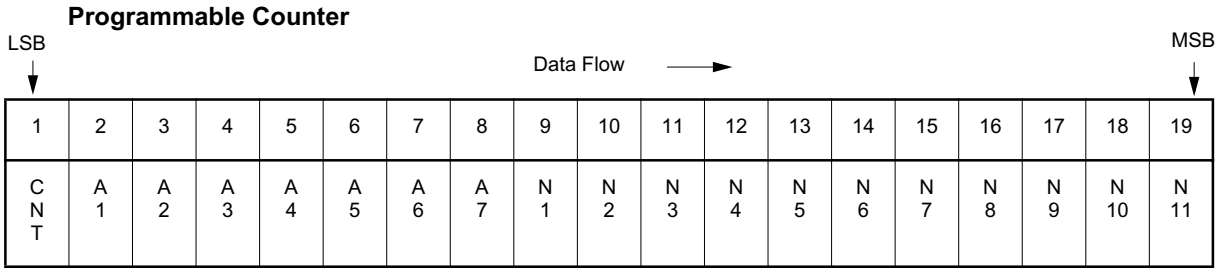
Serial Data Input

Serial data is entered using the Data, Clock and LE pins. The serial data controls the programmable reference counters and the programmable counters separately.

Binary serial data is entered through the Data pin when the LE pin is held low. One bit of data is shifted into the shift register on the rising edge of the Clock. When the LE signal pin is taken high, entered data is latched into the appropriate counters according to the control bit settings as follows:

Functional Descriptions

Shift Register Configuration



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CNT	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CNT	Control bit	[Table 1]
N1 to N11	Divide ratio setting bits for the programmable counter (3 to 2,047)	[Table 3]
A1 to A7	Divide ratio setting bits for the swallow counter (0 to 127)	[Table 4]

Note: Input data with MSB first.

Table 2. Binary 14-Bit Programmable Reference Counter Data Setting

Divide ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table 3. Binary 11-Bit Programmable Counter Data Setting

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Functional Descriptions

Table 4. Binary 7-Bit Swallow Counter Data Setting

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range = 0 to 127

Table 5. Prescaler Data Setting for MB15E03SL, MB15E05SL (SW Bit)

SW	Prescaler Dived Ratio
H	64/65
L	128/129

Prescaler Data Setting for MB15E07SL (SW Bit)

SW	Prescaler Dived Ratio
H	32/33
L	64/65

Relationship Between the FC Input and Phase Characteristics

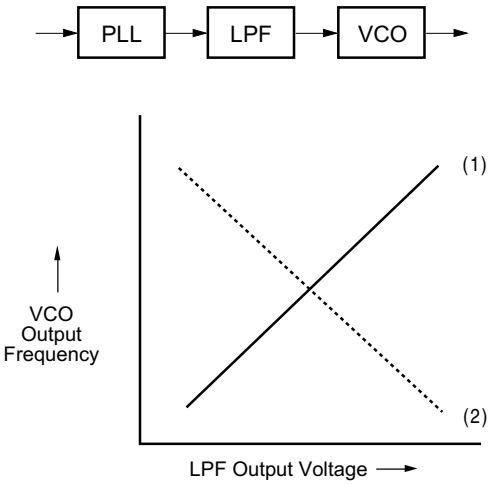
The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (fr, fp) are reversed according to the FC bit setting. Also, the monitor pin (f_{OUT}) output is controlled by the FC bit. The relationship between the FC bit setting and each of D_O, fr, and fp is shown below.

Table 6. FC Bit Data Setting (LDS = "H")

	FC = High				FC = Low			
	Do	fR	fP	LD/fout	Do	fR	fP	LD/fout
$fr > f_P$	H	L	L		L	H	Z*	
$fr < f_P$	L	H	Z*	fout = fr	H	L	L	fout = fp
$fr = f_P$	Z*	L	Z*		Z*	L	Z*	

* High impedance

Functional Descriptions



(1) When the LPF and VCO characteristics are similar to (1), set the FC bit high.

(2) When the VCO characteristics are similar to (2), set the FC bit low.

Table 7. LD/f_{OUT} Output Select Data Setting (LDS Bit)

LDS	LD/f_{OUT} Output Signal
H	f_{OUT} signals
L	LD signals

Table 8. Charge Pump Current Setting (CS Bit)

CS	Current Value
H	± 6.0 mA
L	± 1.5 mA

Table 9. Do Output Impedance Pin Setting (ZC Pin)

CS	Do Output
H	Normal output
L	High impedance

Functional Descriptions

Power-Saving Mode (Intermittent Mode Control)

The Intermittent Mode Control circuit greatly reduces the PLL power consumption by shutting down various internal functions, depending upon the settings of the power-save (PS) pins. (See the Electrical Characteristics chart for the specific value of current when the device is in the power-saving mode.) In this mode, the phase detector output, Do, becomes high impedance.

Setting the PS pin high releases the power-saving mode, returning the selected PLL to normal operation.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation, at which time the phase comparator output signal is unpredictable due to the unknown relationship between the comparison frequency (fp) and the reference frequency (fr). This can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lock-up time.

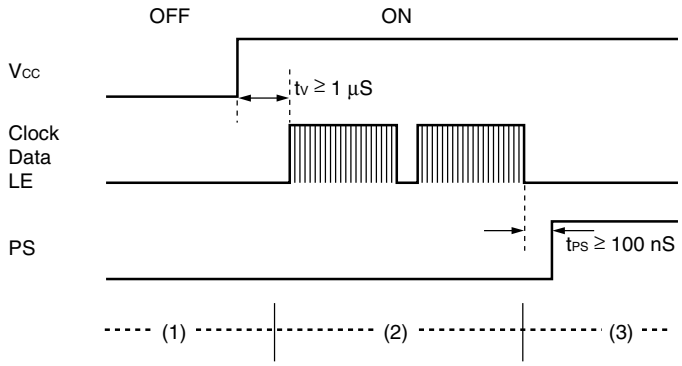
To prevent this the Intermittent Mode Control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

When power (V_{CC}) is first applied, the device must be in standby mode, PS = Low, for at least 1µs.

Table 10. Power Save Pin Setting (PS Pins)

PS Pins	Status
H	Normal mode
L	Power saving mode

Power-ON Timing



(1) PS = L (power-saving mode) at Power ON
(2) Set serial data 1 µs later after power supply remains stable ($V_{CC} \geq 2.2V$).
(3) Release power-saving mode (PS: L → H) 100 ns later after setting serial data.

Serial Data Input Timing

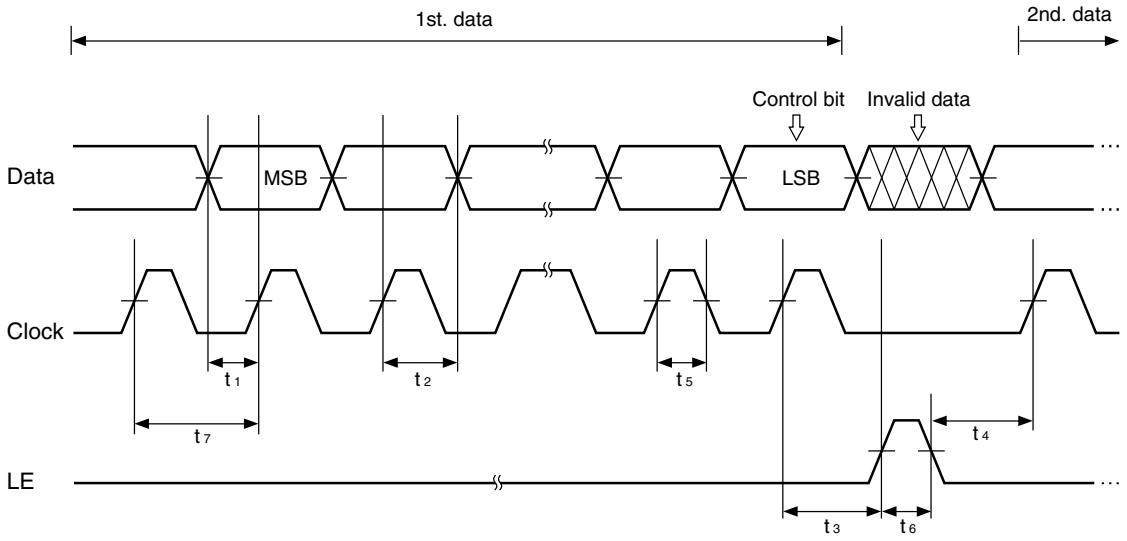


Table 11. Timing Parameters

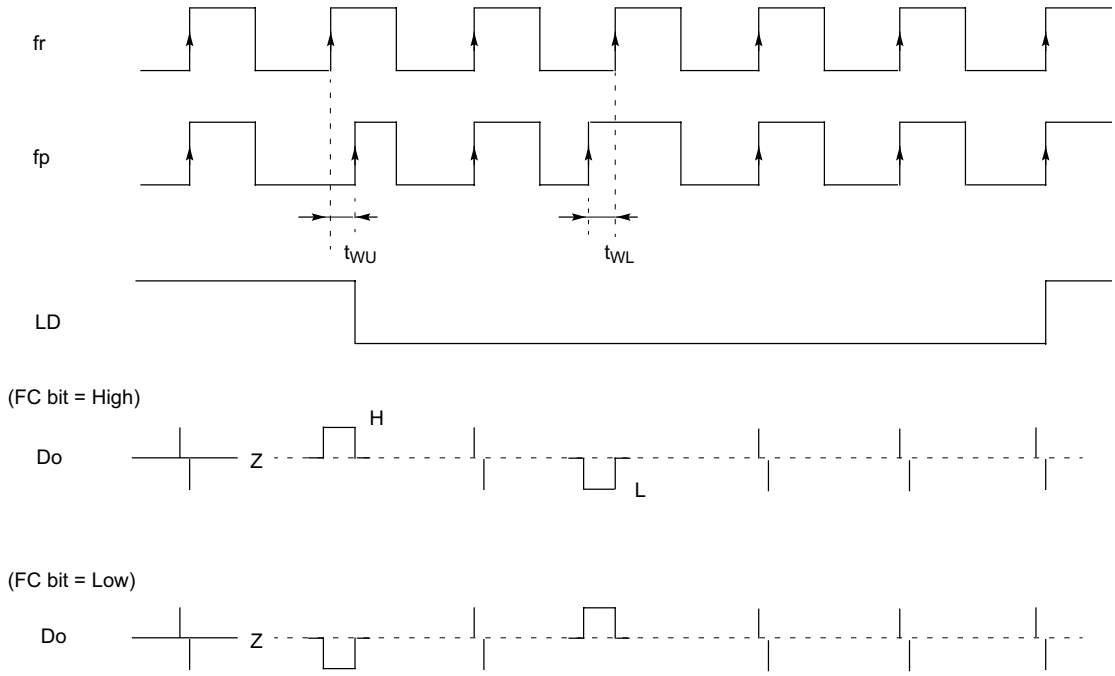
Parameter	Min.	Typ.	Max.	Unit
t1	20	–	–	ns
t2	20	–	–	ns
t3	30	–	–	ns
t4	30	–	–	ns

Parameter	Min.	Typ.	Max.	Unit
t5	100	–	–	ns
t6	20	–	–	ns
t7	100	–	–	ns

On the rising edge of the clock, one bit of the data is transferred into the shift register.

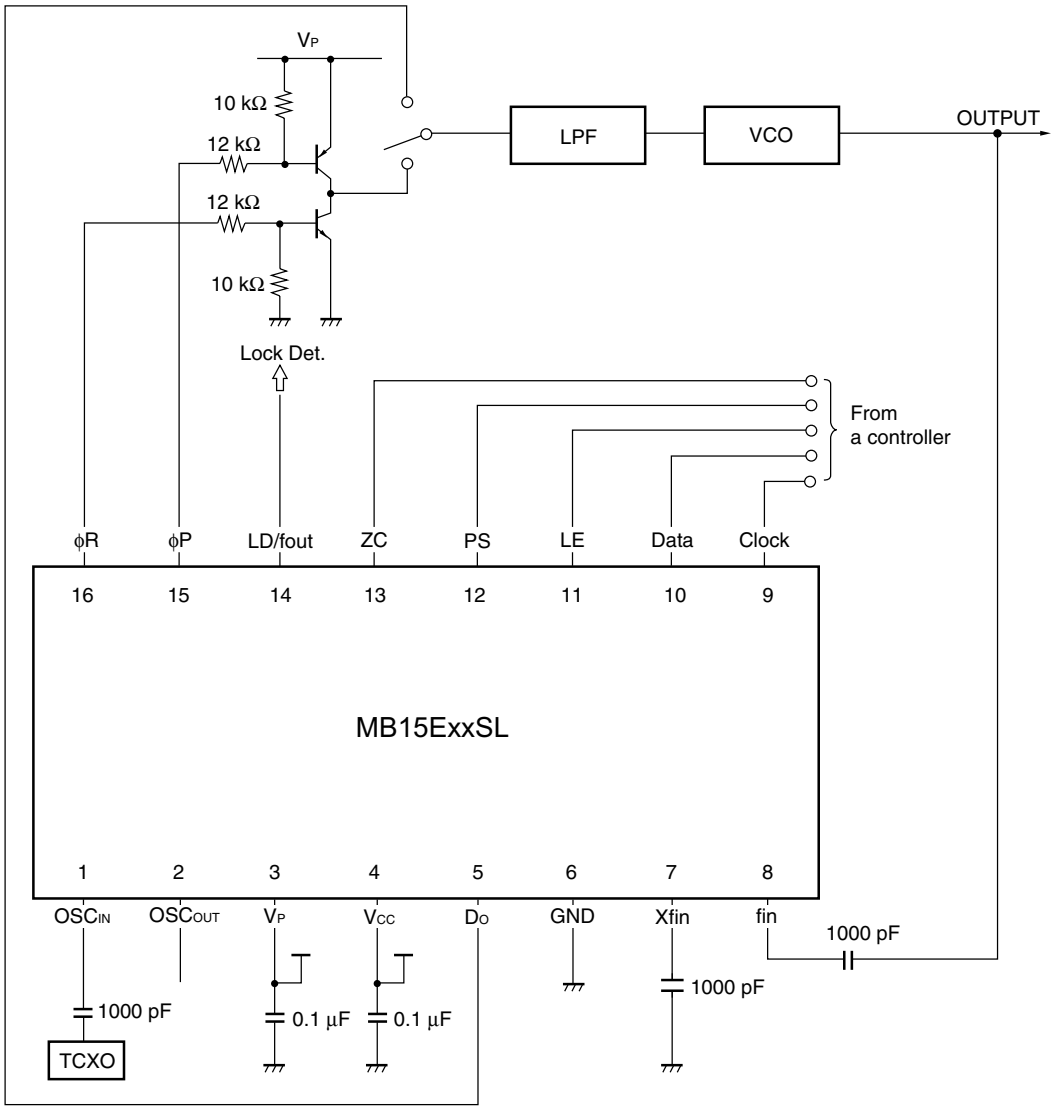
Note: LE should be “L” when the data is transferred into the shift register.

Phase Detector Output Waveform



Notes:
1) Phase error detection range: -2π to $+2\pi$
2) Pulses on Do signal during locked state are output to prevent dead zone.
3) LD output becomes low when phase is t_{WU} or more. LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
4) t_{WU} and t_{WL} depend on OSC_{IN} input frequency.
   $t_{WU} \geq 2/fosc$ (s) (e. g. $t_{WU} \geq 156.3$ns, fosc = 12.8MHz)
   $t_{WU} \leq 4/fosc$ (s) (e. g. $t_{WL} \leq 312.5$ns, fosc = 12.8MHz)
5) LD becomes high during the power-saving mode (PS = "L").

Application Example



V_P: 5.5V Max

Notes: 1) 16-pin SSOP
2) In case of using a crystal resonator, it is necessary to optimize matching between the crystal and this device, and it is advised to perform a detailed system evaluation. It is also recommended to consult with the supplier of the crystal resonator. (The reference oscillator circuit provides its own bias)

Usage Precautions

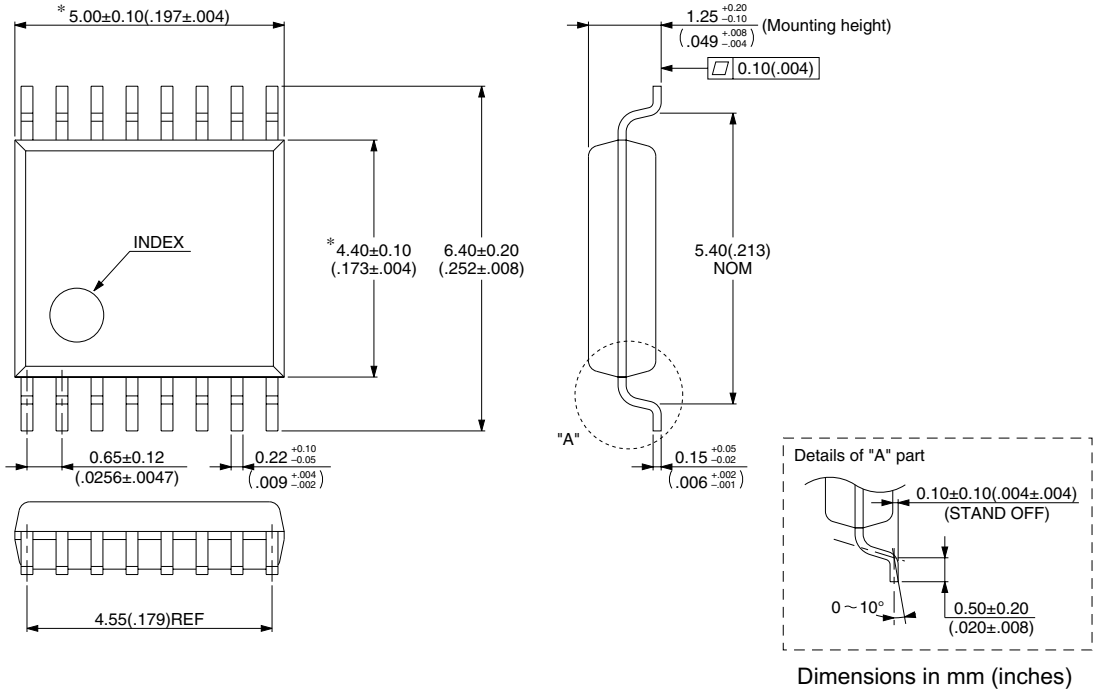
To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet when transporting a board mounted device.

Ordering Information

Part Number	Package
MB15ExxSLPFV1	16 pin, Plastic SSOP (FPT-16P-M05)
MB15ExxSLPV1	16 pin, Plastic BCC (LCC-16P-M06)

Package Dimensions

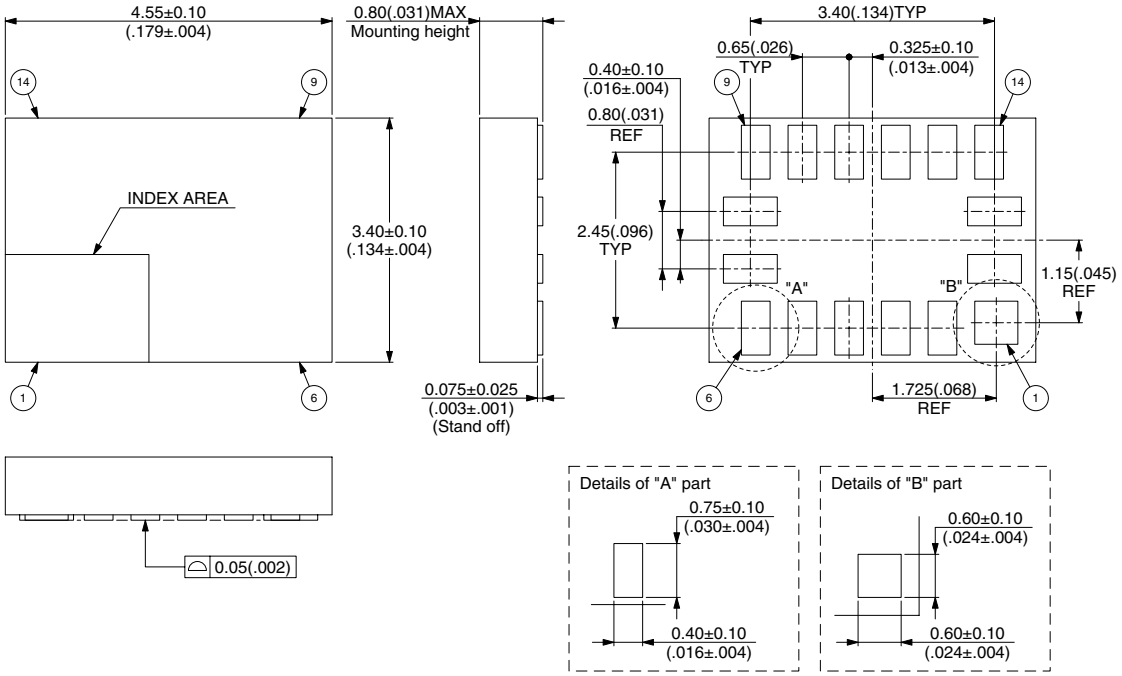


Dimensions in mm (inches)

Note: 16-pin, Plastic SSOP (FPT-16P-M05)

*These dimensions do not include resin protrusion.

Package Dimensions



Dimensions in mm (inches)

Note: 16-pad, Plastic BCC (LCC-16P-M06)

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