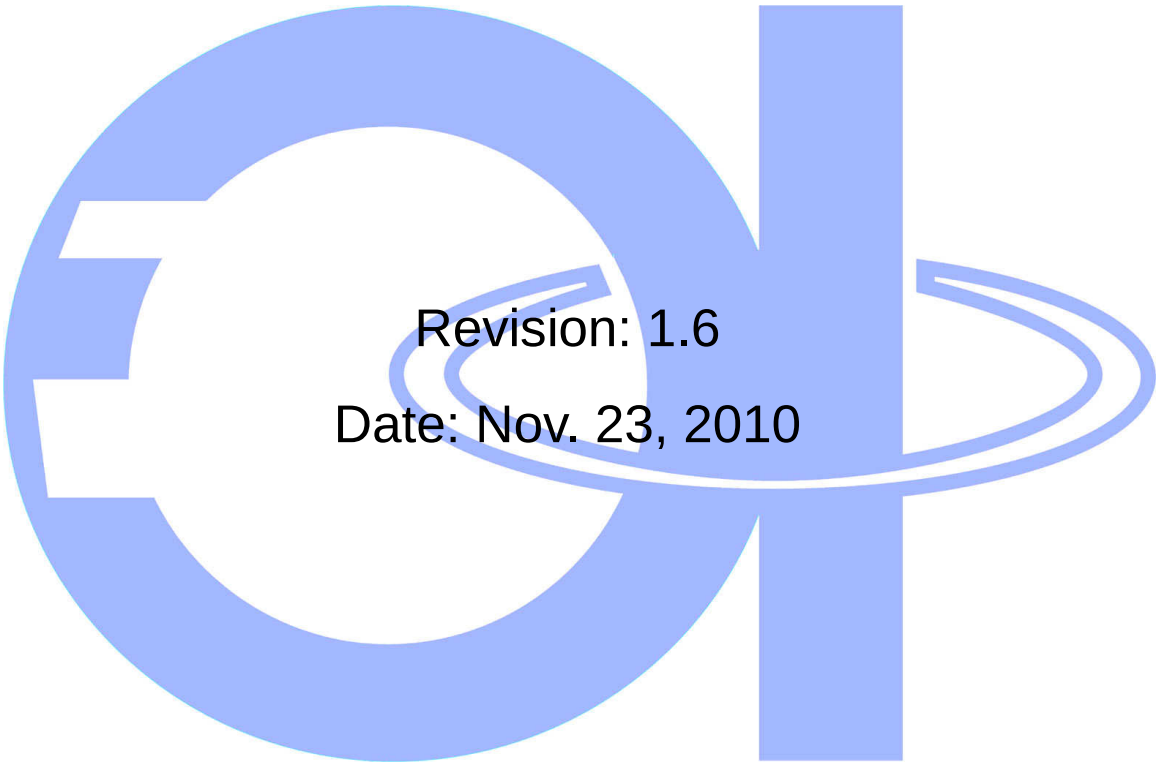
JL4209A

Multimedia Controller



Revision: 1.6

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0. Revision History

Revision	Description of Changes	Date
1.0	First Release	2007/10/26
1.1	Change pin name “I2S_WB” to “I2S_WS” on the pin assignment diagram	2007/11/01
1.2	Add AC Timing Specification	2007/11/12
1.3	1. Modify Pin Description table ● Add GPIO_39 and GPIO_40 to the Memo field ● Remove NF_NCE2, NF_RDY2, NF_NCE3, NF_RDY3, NF_NCE4, NF_RDY4 from the Memo fiels 2. Modify GPIO Mux Table ● Remove PG1_Out_1 from Alt[2:0]= 10 field ● Change name “SD_D4” to “MMC_D4” in the Alt[2:0]= 01 field ● Change name “SD_D5” to “MMC_D5” in the Alt[2:0]= 01 field ● Change name “SD_D6” to “MMC_D6” in the Alt[2:0]= 01 field ● Change name “SD_D7” to “MMC_D7” in the Alt[2:0]= 01 field ● Remove NF_NCE2, NF_RDY2, NF_NCE3, NF_RDY3, NF_NCE4, NF_RDY4 in the Alt[2:0]= 10 field ● Remove Ext_Clk_Out in the Alt[2:0]= 11 field ● Remove AC97 signals 3. Change name “PG1_Out_1” to PG1_Out_0” in the Alt[2:0]= 01 field 4. Change name “I2S_DATAO” to “I2S_DO “ in the Alt[2:0]= 01 field 5. Change name “SCL” to “I2C_SCL” in the Alt[2:0]= 01 field 6. Change name “SDA” to “I2C_SDA” in the Alt[2:0]= 01 field 7. Change name “IR_In_0” to “IR_DI” in the Alt[2:0]= 01 field 8. Change name “SPI_nCS_0” to “SPI_NCS“ in the Alt[2:0]= 01 field 9. Change title name “RGB delta” to “Serial RGB”, “RGB Stipe” to “Without TCON”, and “Digital TCON” to “With TCON” in the DDI (Digital Display Interface) Table 10. Change name TCON_R0~R5 to LCD_R0~R5, TCON_G0~G5 to LCD_G0~G5 and TCON_B0~B5 to LCD_B0~B5 in the DDI (Digital Display Interface) Table 11. Remove Analog_LCD field from the DDI (Digital Display Interface) Table 12. Change iROM to the internal ROM (iROM) in the Booting table 13. Change name LCD_Data0~7 to LCD_D0~7 int the DDI (Digital Display Interface) Table 14. Change “Video Frame Rate：QVGA@60fps、VGA@30fps” to “Video	2007/12/11

	Frame Rate：up to VGA@30fps”	
1.4	1. Rename pin 54 to USB_REF. 2. Modify block diagram in chapter 3. 3. Modify the diagram in chapter 5.1. 4. Correct the dimension in PQFP-208 package. 5. Rename chapter 9 to “CHIP REVISION HISTORY”.	2008/05/14
1.5	1. Remove following display features in paragraph 2. ● Embedded three 10-bit video DACs for TV display or S-video output ● CCIR601/656 input interface 2. Modify Block Diagram in paragraph 3. ● Remove CCIR601/656 input interface.	2008/05/28

1. General Description

JL4209A is a multi-media system on chip (SoC) designed and developed by Jeilin Technology, Taiwan. With LCD of different size, JL4209A can be applied to make digital photo frame. Jeilin Technology will provide complete system design to allow client or distributor enter easier and earlier the digital photo frame market.

JL4209A digital photo frame can playback photos (JPEG), movie (Motion JPEG), and music (MP3) from memory card or built-in memory. This will allow user to directly view and share photos and listen to music without developing the photos for viewing later. JL4209A digital photo frame has added many functions that traditional photo frame does not have, for example, auto slide browsing, music playing in the background while photo browsing, transition effects while photo browsing, clock, alarm clock, and calendar. All these functions can be achieved without using a computer.

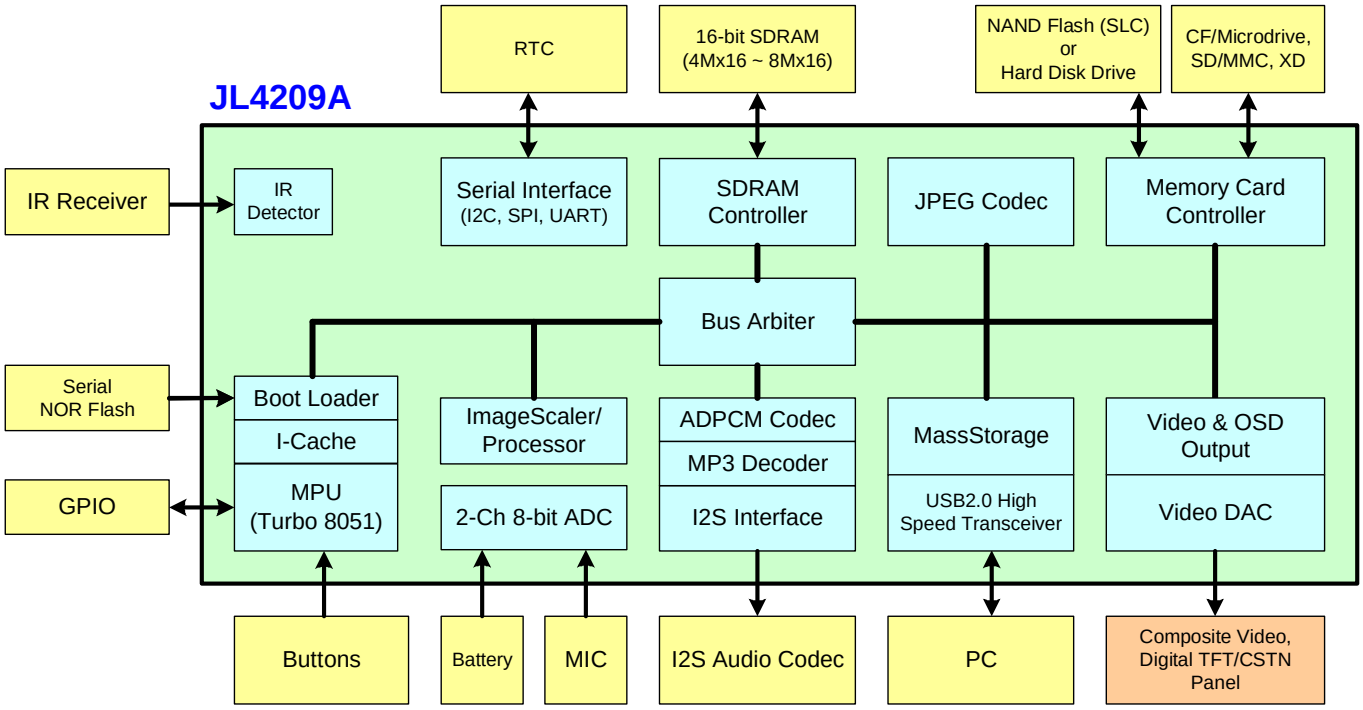
2. Features

- USB Interface
  - High-speed USB 2.0 device function with embedded PHY
  - Supports Mass-Storage Class (MSC)
  - Supports PictBridge interface (direct picture print)
- Storage Media
  - CompactFlash Interface
    - Complies with CF+ and CompactFlash Specification Revision 3.0
  - IDE Interface
    - Complies with ATA /ATAPI-6 Specification Rev 2.0
    - Supports PIO mode 0~4, Multiword DMA mode 0~2, and Ultra DMA mode 0~5
  - SD/MMC Interface
    - Complies with SD 2.0
    - Complies with MMC 4.0
  - NAND Flash/XD/SmartMedia Interface
- Display Feature
  - Embedded TV Encoder (NTSC/PAL) to output CVBS (Composite Video).
  - Supports digital RGB TFT-LCD panel
  - Supports RGB565/666/888 formats
  - Supports smaller size TFT-LCD panel with CPU interface
  - Supports 8-bit CCIR601/656 output interface
- OSD Feature
  - Font-based OSD
  - Graphic-based OSD

- Audio Feature
  - 8/16-bit PCM, 4-bit IMA-ADPCM audio codec
  - Inter-IC Sound (I^2S) interface
  - Embedded 2 channels of 8-bit ADC for voice record, battery detect or other applications
- MP3 Feature
  - Built-in MP3 decoder engine
  - Supports both ISO 11172-3 and ISO 13818-3 layer III audio decoding
  - Supports 8 KHz, 11.025 KHz, 12 KHz,16 KHz, 22.05 KHz, 24 KHz, 32 KHz, 44.1 KHz, 48 KHz sampling rate
  - Ten-band equalizer with 64 steps for -20 to 20 dB gain.
  - Photo slide show with MP3 background playback.
- JPEG codec
  - Supports photo resolution up to 16,384 x 16,384 pixels
  - High-speed JPEG compression/decompression rate: 27M Pixel/sec
  - Supports non-progressive JPEG
  - Supports baseline JPEG format
  - Supports thumbnail decoding
- Video Playback
  - File Format：Only Support Motion JPEG
  - Audio Signal：PCM Format、ADPCM Format
  - Video Frame Rate：up to VGA@30fps
  - Supports video scaling and Picture-In-Picture functions
- SDRAM interface
  - Supports 16-bit SDRAM up to 8Mx16 bits
- Image Display Functions
  - Preview, Slide Show, Zoom, Pan, Rotate, and so on
  - Image Rotation: 0, 90, 180, or 270 degree in clockwise or counter-clockwise direction
  - Image scale function to fit screen
  - Picture In Picture display
  - Transition Effect in photo playback
- Embedded Turbo 8051
  - Supports ISP Function: It's easy-to-use function to upgrade the system firmware directly from memory cards or USB port.
  - Provides lots of GPIOs
- Provides UART, SPI-master and I^2C-master serial ports
- Remote control

- Package
  - 208-pin PQFP

3. Block Diagram

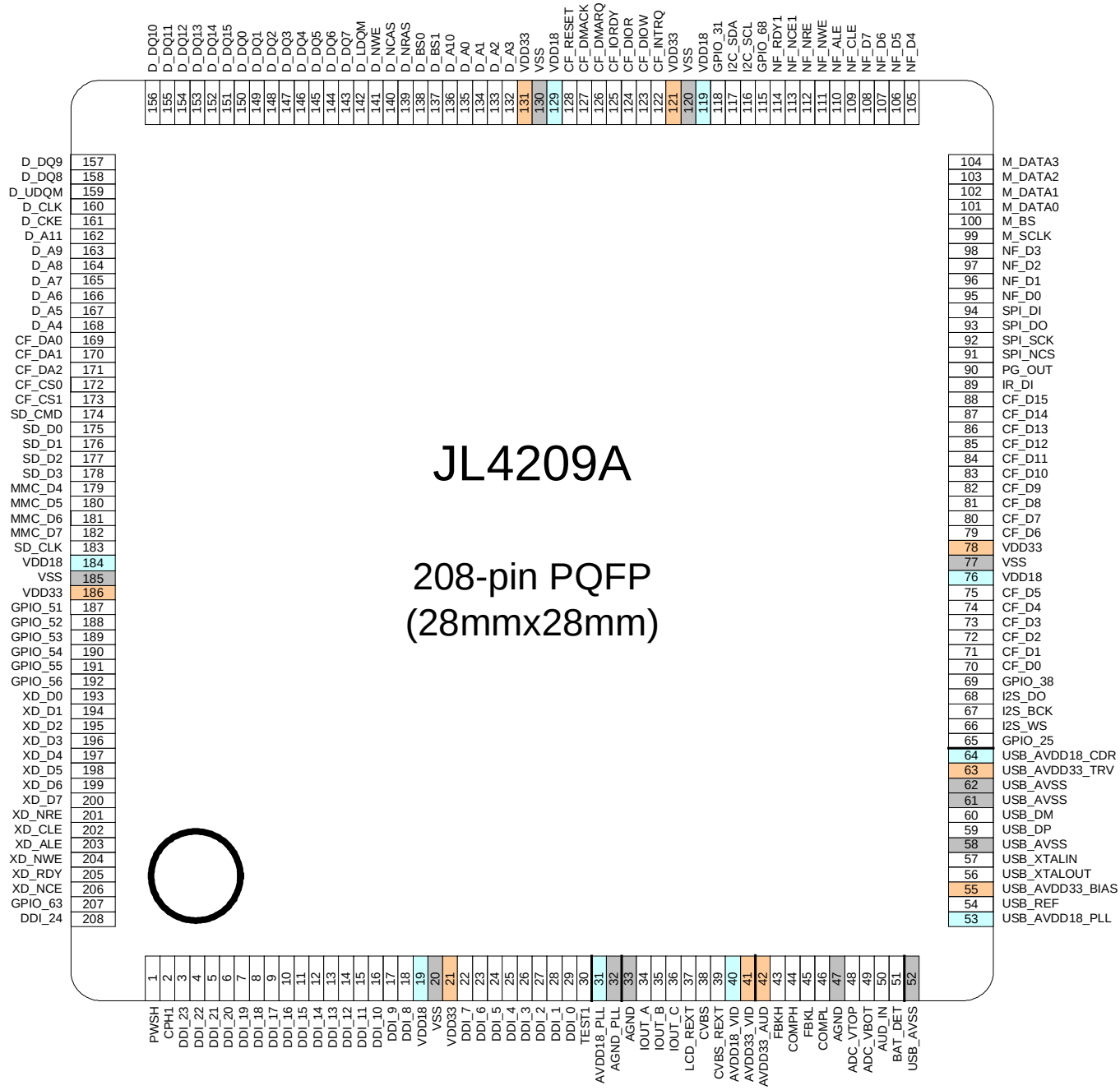


4. Applications

- Digital Photo Frame (DPF)
  - Viewing Photos (JPEG)
  - Viewing Movie (Motion JPEG AVI)
  - Listening to MP3 music
- USB2.0 Card Reader
- DPF with Clock/Calendar

5. Pin Assignment and Pin Description

5.1 Pin Assignment



5.2 Pin Description

Pin #	Pin name	Type	Description	Memo
1	PWSH	O24	Reserved pin	
2	CPH1	O24	Sampling and shifting clock pulse for data drive for TFT TCON.(24mA driving ability)	
3	DDI_23	O2	Digital Display Interface #23	GPIO_23
4	DDI_22	O2	Digital Display Interface #22	GPIO_22
5	DDI_21	O2	Digital Display Interface #21	GPIO_21
6	DDI_20	O2	Digital Display Interface #20	GPIO_20
7	DDI_19	O2	Digital Display Interface #19	GPIO_19
8	DDI_18	O2	Digital Display Interface #18	GPIO_18
9	DDI_17	O2	Digital Display Interface #17	GPIO_17
10	DDI_16	O2	Digital Display Interface #16	GPIO_16
11	DDI_15	O2	Digital Display Interface #15	GPIO_15
12	DDI_14	O2	Digital Display Interface #14	GPIO_14
13	DDI_13	O2	Digital Display Interface #13	GPIO_13
14	DDI_12	O2	Digital Display Interface #12	GPIO_12
15	DDI_11	O2	Digital Display Interface #11	GPIO_11
16	DDI_10	O2	Digital Display Interface #10	GPIO_10
17	DDI_9	O2	Digital Display Interface #9	GPIO_9
18	DDI_8	O2	Digital Display Interface #8	GPIO_8
19	VDD18	P	Core power 1.8V	
20	VSS	G	Ground	
21	VDD33	P	Pad power 3.3V	
22	DDI_7	O2	Digital Display Interface #7	GPIO_7
23	DDI_6	O2	Digital Display Interface #6	GPIO_6
24	DDI_5	O2	Digital Display Interface #5	GPIO_5
25	DDI_4	O2	Digital Display Interface #4	GPIO_4
26	DDI_3	O2	Digital Display Interface #3	GPIO_3
27	DDI_2	O2	Digital Display Interface #2	GPIO_2
28	DDI_1	O2	Digital Display Interface #1	GPIO_1
29	DDI_0	O2	Digital Display Interface #0	GPIO_0
30	TEST1	I	Reserved pin, which must be pull-high with a 10K ohms resistor	
31	AVDD18_PLL	P	PLL power 1.8V	
32	AGND_PLL	G	PLL ground	

Pin #	Pin name	Type	Description	Memo
33	AGND	G	Analog ground	
34	IOOUT_A	A	Reserved pin	
35	IOOUT_B	A	Luminance output of S-Video	
36	IOOUT_C	A	Chroma output of S-Video	
37	DAC_REXT	A	The reference current for the video DAC.This pin should connect a resistor to ground. The output current I =128*1.25/Rext (mA)	
38	CVBS	A	Composite video signal output	
39	CVBS_REXT	A	The reference current for the video DAC. This pin should connect a resistor to ground. The output current I =128*1.25/Rext(mA)	
40	AVDD18_VID	P	Video DAC power 1.8V	
41	AVDD33_VID	P	Video DAC power 3.3V	
42	AVDD33_AUD	P	ADC/DAC power 3.3V	
43	FBKH	A	Reserved pin	
44	COMPH	A	Reserved pin	
45	FBKL	A	Reserved pin	
46	COMPL	A	Reserved pin	
47	AGND	G	Analog ground	
48	ADC_VTOP	A	Reference voltage decoupling for audio ADC. The nominal value is 2.7V. It should be connected an 0.1uF capacitor to ground	
49	ADC_VBOT	A	Reference voltage decoupling for audio ADC. The nominal value is 1.2V. It should be connected an 0.1uF capacitor to ground	
50	AUD_IN	A	Audio signal input	
51	ADC_IN	A	Analog signal input for ADC.	
52	USB_AVSS	G	USB transceiver ground	
53	USB_AVDD18_PLL	P	USB PLL power 1.8V	
54	USB_REF	A	Connect 12.1Kohm (1%) resistor to ground. The purpose of RES is to provide a reference for the current resource of the high-speed driver.	
55	USB_AVDD33_BIAS	P	3.3V power for BIAS	
56	USB_XTALOUT	A	Oscillator output. Connect to a 12Mhz crystal	
57	USB_XTALIN	A	Oscillator input. Connect to a 12Mhz crystal	

Pin #	Pin name	Type	Description	Memo
58	USB_AVSS	G	USB transceiver ground	
59	USB_DP	A	USB D+	
60	USB_DM	A	USB D-	
61	USB_AVSS	G	USB transceiver ground	
62	USB_AVSS	G	USB transceiver ground	
63	USB_AVDD33_TRV	P	3.3V power for USB transceiver	
64	USB_AVDD18_CDR	P	1.8V power for CDR	
65	GPIO_25	B2	General purpose I/O #25	
66	I2S_WS	O2	I^2S word select output	GPIO_26
67	I2S_BCK	O2	I^2S serial clock output	GPIO_27
68	I2S_DO	O2	I^2S serial data output	GPIO_28
69	GPIO_38	B2	General purpose I/O #38	
70	CF_D0	B4	CF data bus 0	
71	CF_D1	B4	CF data bus 1	
72	CF_D2	B4	CF data bus 2	
73	CF_D3	B4	CF data bus 3	
74	CF_D4	B4	CF data bus 4	
75	CF_D5	B4	CF data bus 5	
76	VDD18	P	Core power 1.8V	
77	VSS	G	Ground	
78	VDD33	P	Pad power 3.3V	
79	CF_D6	B4	CF data bus 6	
80	CF_D7	B4	CF data bus 7	
81	CF_D8	B4	CF data bus 8	
82	CF_D9	B4	CF data bus 9	
83	CF_D10	B4	CF data bus 10	
84	CF_D11	B4	CF data bus 11	
85	CF_D12	B4	CF data bus 12	
86	CF_D13	B4	CF data bus 13	
87	CF_D14	B4	CF data bus 14	
88	CF_D15	B4	CF data bus 15	
89	IR_DI	I	Data input of remote control	GPIO_32
90	PG_OUT	O2	PWM signal output for backlight brightness control	GPIO_33
91	SPI_NCS	O2	SPI chip select, active low	GPIO_34
92	SPI_SCK	O2	SPI serial clock output	GPIO_35

Pin #	Pin name	Type	Description	Memo
93	SPI_DO	O2	SPI serial data output	GPIO_36
94	SPI_DI	I	SPI serial data input	GPIO_37
95	NF_D0	B4	Data 0 of NAND Flash memory	
96	NF_D1	B4	Data 1 of NAND Flash memory	
97	NF_D2	B4	Data 2 of NAND Flash memory	
98	NF_D3	B4	Data 3 of NAND Flash memory	
99	M_SCLK	O8	Memory Clock Output	GPIO_57
100	M_BS	O4	Memory Bus State Output	GPIO_58
101	M_DATA0	B4	Memory Parallel Data Line 0.	GPIO_59
102	M_DATA1	B4	Memory Parallel Data Line 1.	GPIO_60
103	M_DATA2	B4	Memory Parallel Data Line 2.	GPIO_61
104	M_DATA3	B4	Memory Parallel Data Line 3.	GPIO_62
105	NF_D4	B4	Data 4 of NAND Flash memory	
106	NF_D5	B4	Data 5 of NAND Flash memory	
107	NF_D6	B4	Data 6 of NAND Flash memory	
108	NF_D7	B4	Data 7 of NAND Flash memory	
109	NF_CLE	O4	Command latch enable for NAND Flash memory	
110	NF_ALE	O4	Address latch enable for NAND Flash memory	
111	NF_NWE	O4	Write strobe for NAND Flash memory	
112	NF_NRE	O4	Read strobe for NAND Flash memory	
113	NF_NCE1	O4	Chip enable signal for the 1st die on NAND Flash	GPIO_39
114	NF_RDY1	I	Ready signal of the 1st die on NAND Flash	GPIO_40
115	GPIO_68	B2	General purpose I/O #68	
116	I2C_SCL	OD	I2C serial clock output	GPIO_29
117	I2C_SDA	BD	I2C serial data	GPIO_30
118	GPIO_31	B2	General purpose I/O #31	
119	VDD18	P	Core power 1.8V	
120	VSS	G	Ground	
121	VDD33	P	Pad power 3.3V	
122	CF_INTRQ	I	CF Interrupt Request	
123	CF_DIOW	O4	CF read strobe output	
124	CF_DIOR	O4	CF write strobe output	
125	CF_IORDY	I	CF card ready	
126	CF_DMARQ	O4	DMA acknowledge signal in true IDE mode.	
127	CF_DMACK	O4	DMA request signal in true IDE mode.	

Pin #	Pin name	Type	Description	Memo
128	CF_RESET	O4	Hardware Reset output	
129	VDD18	P	Core power 1.8V	
130	VSS	G	Ground	
131	VDD33	P	Pad power 3.3V	
132	D_A3	O8	SDRAM address bus 3, which must be pull-high with a 10K ohm resistor for normal operation	
133	D_A2	O8	SDRAM address bus 2, which must be pull-high with a 10K ohm resistor for normal operation	
134	D_A1	O8	SDRAM address bus 1	Boot_Mode[1] *__Note 1__
135	D_A0	O8	SDRAM address bus 0	Boot_Mode[0] *__Note 1__
136	D_A10	O8	SDRAM address bus 10	Latch_in(6), Key_in(22)
137	D_BS1	O8	SDRAM bank address 1	
138	D_BS0	O8	SDRAM bank address 0	
139	D_NRAS	O8	SDRAM raw address strobe output	
140	D_NCAS	O8	SDRAM column address strobe output	
141	D_NWE	O8	SDRAM write strobe	
142	D_LDQM	O8	SDRAM low byte data write mask	
143	D_DQ7	B8	SDRAM data bus 7	Key_in(7)
144	D_DQ6	B8	SDRAM data bus 6	Key_in(6)
145	D_DQ5	B8	SDRAM data bus 5	Key_in(5)
146	D_DQ4	B8	SDRAM data bus 4	Key_in(4)
147	D_DQ3	B8	SDRAM data bus 3	Key_in(3)
148	D_DQ2	B8	SDRAM data bus 2	Key_in(2)
149	D_DQ1	B8	SDRAM data bus 1	Key_in(1)
150	D_DQ0	B8	SDRAM data bus 0	Key_in(0)
151	D_DQ15	B8	SDRAM data bus 15	Key_in(15)
152	D_DQ14	B8	SDRAM data bus 14	Key_in(14)
153	D_DQ13	B8	SDRAM data bus 13	Key_in(13)
154	D_DQ12	B8	SDRAM data bus 12	Key_in(12)
155	D_DQ11	B8	SDRAM data bus 11	Key_in(11)
156	D_DQ10	B8	SDRAM data bus 10	Key_in(10)
157	D_DQ9	B8	SDRAM data bus 9	Key_in(9)

Pin #	Pin name	Type	Description	Memo
158	D_DQ8	B8	SDRAM data bus 8	Key_in(8)
159	D_UDQM	O8	SDRAM high byte data write mask	
160	D_CLK	O8	SDRAM clock	
161	D_CKE	O8	SDRAM clock enable	
162	D_A11	O8	SDRAM address bus 11	Latch_in(7), Key_in(23)
163	D_A9	O8	SDRAM address bus 9	Latch_in(5), Key_in(21)
164	D_A8	O8	SDRAM address bus 8	Latch_in(4), Key_in(20)
165	D_A7	O8	SDRAM address bus 7	Latch_in(3), Key_in(19)
166	D_A6	O8	SDRAM address bus 6	Latch_in(2), Key_in(18)
167	D_A5	O8	SDRAM address bus 5	Latch_in(1), Key_in(17)
168	D_A4	O8	SDRAM address bus 4	Latch_in(0), Key_in(16)
169	CF_DA0	O4	CF Address Line 0	
170	CF_DA1	O4	CF Address Line 1	
171	CF_DA2	O4	CF Address Line 2	
172	CF_CS0	O4	CF Chip Select 0 in true IDE mode	
173	CF_CS1	O4	CF Chip Select 1 in true IDE mode	
174	SD_CMD	B4	Command signal for SD/MMC	GPIO_42
175	SD_D0	B4	Data bit 0 of SD/MMC	GPIO_43
176	SD_D1	B4	Data bit 1 of SD/MMC	GPIO_44
177	SD_D2	B4	Data bit 2 of SD/MMC	GPIO_45
178	SD_D3	B4	Data bit 3 of SD/MMC	GPIO_46
179	MMC_D4	B4	Data bit 4 of MMC	GPIO_47
180	MMC_D5	B4	Data bit 5 of MMC	GPIO_48
181	MMC_D6	B4	Data bit 6 of MMC	GPIO_49
182	MMC_D7	B4	Data bit 7 of MMC	GPIO_50
183	SD_CLK	O8	Clock signal for SD/MMC	GPIO_41
184	VDD18	P	Core power 1.8V	
185	VSS	G	Ground	

Pin #	Pin name	Type	Description	Memo
186	VDD33	P	Pad power 3.3V	
187	GPIO_51	B2	General purpose I/O # 51	
188	GPIO_52	B2	General purpose I/O # 52	
189	GPIO_53	B2	General purpose I/O # 53	
190	GPIO_54	B2	General purpose I/O # 54	
191	GPIO_55	B2	General purpose I/O # 55	
192	GPIO_56	B2	General purpose I/O # 56	
193	XD_D0	B4	Data bit 0 of XD	
194	XD_D1	B4	Data bit 1 of XD	
195	XD_D2	B4	Data bit 2 of XD	
196	XD_D3	B4	Data bit 3 of XD	
197	XD_D4	B4	Data bit 4 of XD	
198	XD_D5	B4	Data bit 5 of XD	
199	XD_D6	B4	Data bit 6 of XD	
200	XD_D7	B4	Data bit 7 of XD	
201	XD_NRE	O4	Read strobe for XD	
202	XD_CLE	O4	Command latch enable for XD	
203	XD_ALE	O4	Address latch enable for XD	
204	XD_NWE	O4	Write strobe for XD	
205	XD_RDY	O4	Ready signal for XD	
206	XD_NCE	O4	Chip enable signal for XD	
207	GPIO_63	B16	General purpose I/O # 63	
208	DDI_24	O2	Digital Display Interface # 24	GPIO_24

NOTE:

*1: Pull up/down these two pins with 10K ohm resistor to select system booting method.

Booting Mode	Function
00	Booting from the internal ROM (iROM)
01	Booting from Serial NOR Flash
10	Booting from Parallel NOR Flash
11	Booting from NAND Flash memory

*2: All digital input pin can take 5V tolerance

Type	Description
P	Power pin
G	Ground pin
A	Analog pin
I	3.3V CMOS input pin
O	3.3V CMOS output pin with 4mA driving ability
O8	3.3V CMOS output pin with 8mA driving ability
O24	3.3V CMOS output pin with 24mA driving ability
B	3.3V CMOS bi-direction pin with 2mA driving ability
B4	3.3V CMOS bi-direction pin with 4mA driving ability
B8	3.3V CMOS bi-direction pin with 8mA driving ability
B16	3.3V CMOS bi-direction pin with 16mA driving ability
BD	3.3V CMOS bi-direction pin with open drian output pin
OD	3.3V CMOS open drain output pin

5.3 GPIO Mux Table

NOTE: Each GPIO pin has its own function select registers, Alt[2:1], firmware can configure each GPIO pin to different function individually.

Alt[2:1]= 00		Alt[2:1]= 01		Alt[2:1]= 10		Alt[2:1]= 11	
GPIO_0	B	DDI_0	O	-		-	
GPIO_1	B	DDI_1	O	-		-	
GPIO_2	B	DDI_2	O	-		-	
GPIO_3	B	DDI_3	O	-		-	
GPIO_4	B	DDI_4	O	-		-	
GPIO_5	B	DDI_5	O	-		-	
GPIO_6	B	DDI_6	O	-		-	
GPIO_7	B	DDI_7	O	-		-	
GPIO_8	B	DDI_8	O	-		-	
GPIO_9	B	DDI_9	O	-		-	
GPIO_10	B	DDI_10	O	-		-	
GPIO_11	B	DDI_11	O	CCIR601_In_CLK	I	-	
GPIO_12	B	DDI_12	O	CCIR601_In_D0	I	-	
GPIO_13	B	DDI_13	O	CCIR601_In_D1	I	-	
GPIO_14	B	DDI_14	O	CCIR601_In_D2	I	-	
GPIO_15	B	DDI_15	O	CCIR601_In_D3	I	-	
GPIO_16	B	DDI_16	O	CCIR601_In_D4	I	-	
GPIO_17	B	DDI_17	O	CCIR601_In_D5	I	-	
GPIO_18	B	DDI_18	O	CCIR601_In_D6	I	UART_TX	O
GPIO_19	B	DDI_19	O	CCIR601_In_D7	I	UART_RX	I
GPIO_20	B	DDI_20	O	CCIR601_In_HSYNC	I	-	
GPIO_21	B	DDI_21	O	CCIR601_In_VSYNC	I	-	
GPIO_22	B	DDI_22	O	-		-	
GPIO_23	B	DDI_23	O	-		-	
GPIO_24	B	DDI_24	O	-		-	
GPIO_25	B	-		-		-	
GPIO_26	B	I2S_WS	O	-		-	
GPIO_27	B	I2S_BCK	O	-		-	
GPIO_28	B	I2S_DO	O	-		-	
GPIO_29	B	I2C_SCL	OD	-		-	
GPIO_30	B	I2C_SDA	OD	-		-	
GPIO_31	B	-		PG1_Out_0	O	-	

Alt[2:1]= 00		Alt[2:1]= 01		Alt[2:1]= 10		Alt[2:1]= 11	
GPIO_32	B	IR_DI	I	-		-	
GPIO_33	B	SPI_nCS_1	O	PWM Signal Output	O	-	
GPIO_34	B	SPI_NCS	O	-		-	
GPIO_35	B	SPI_SCK	O	-		-	
GPIO_36	B	SPI_DO	O	UART_TX	O	-	
GPIO_37	B	SPI_DI	I	UART_RX	I	-	
GPIO_38	B	-		-		-	
GPIO_39	B	NF_nCE1	O	-		-	
GPIO_40	B	NF_RDY1	I	PWM Signal Output	O	-	
GPIO_41	B	SD_CLK	O	-		-	
GPIO_42	B	SD_CMD	O	-		-	
GPIO_43	B	SD_D0	B	-		-	
GPIO_44	B	SD_D1	B	-		-	
GPIO_45	B	SD_D2	B	-		-	
GPIO_46	B	SD_D3	B	-		-	
GPIO_47	B	MMC_D4	B	-		-	
GPIO_48	B	MMC_D5	B	-		-	
GPIO_49	B	MMC_D6	B	-		-	
GPIO_50	B	MMC_D7	B	-		-	
GPIO_51	B	-		-		-	
GPIO_52	B	-		-			
GPIO_53	B	-		-		DDI_25	O
GPIO_54	B	-		-		DDI_26	O
GPIO_55	B	-		-		DDI_27	O
GPIO_56	B	-		-		-	
GPIO_57	B	M_SCLK	O	-		-	
GPIO_58	B	M_BS	O	-		-	
GPIO_59	B	M_DATA0	B	-		-	
GPIO_60	B	M_DATA1	B	-		-	
GPIO_61	B	M_DATA2	B	-		-	
GPIO_62	B	M_DATA3	B	-		-	
GPIO_63	B	PG1_Out_0	O	-		-	
GPIO_68	B	-		-		-	

5.4 DDI (Digital Display Interface) Table

DDI_Mux[2:0] / DDI Pin	0	1	2
	Digital-LCD (Serial RGB)	Digital-LCD (Without TCON)	Digital-LCD (With TCON)
DDI_0	LCD_CLK	LCD_CLK	TCON_CPH1
DDI_1	LCD_HSYNC	LCD_HSYNC	TCON_STV
DDI_2	LCD_VSYNC	LCD_VSYNC	TCON_CKV
DDI_3	LCD_D0	LCD_ENAB	TCON_POL
DDI_4	LCD_D1	LCD_R2	LCD_R0
DDI_5	LCD_D2	LCD_R3	LCD_R1
DDI_6	LCD_D3	LCD_R4	LCD_R2
DDI_7	LCD_D4	LCD_R5	LCD_R3
DDI_8	LCD_D5	LCD_R6	LCD_R4
DDI_9	LCD_D6	LCD_R7	LCD_R5
DDI_10	LCD_D7	LCD_G2	LCD_G0
DDI_11	LCD_H_Ref	LCD_G3	LCD_G1
DDI_12	-	LCD_G4	LCD_G2
DDI_13	-	LCD_G5	LCD_G3
DDI_14	-	LCD_G6	LCD_G4
DDI_15	-	LCD_G7	LCD_G5
DDI_16	-	LCD_B2	LCD_B0
DDI_17	-	LCD_B3	LCD_B1
DDI_18	-	LCD_B4	LCD_B2
DDI_19	-	LCD_B5	LCD_B3
DDI_20	-	LCD_B6	LCD_B4
DDI_21	-	LCD_B7	LCD_B5
DDI_22	-	LCD_R1	TCON_OEH
DDI_23	-	LCD_G1	TCON_STH
DDI_24	-	LCD_B1	TCON_OEV
DDI_25	-	LCD_R0	-
DDI_26	-	LCD_G0	-
DDI_27	-	LCD_B0	-

5.5 NAND Flash and IDE Mux Table

Pin Name		NFIDE_Sel_NF*1=0			NFIDE_Sel_NF=1 (Default)	
NF_D0	B	IDE_INTRQ		I	NF_D0	B
NF_D1	B	IDE_CS0		O	NF_D1	B
NF_D2	B	IDE_CS1		O	NF_D2	B
NF_D3	B	IDE_IORDY		I	NF_D3	B
NF_D4	B	IDE_DA0		O	NF_D4	B
NF_D5	B	IDE_DA1		O	NF_D5	B
NF_D6	B	IDE_DA2		O	NF_D6	B
NF_D7	B	IDE_DMARQ		I	NF_D7	B
NF_CLE	O	IDE_DMACK		O	NF_CLE	O
NF_ALE	O	IDE_RESET		O	NF_ALE	O
NF_NWE	O	IDE_DIOW		O	NF_NWE	O
NF_NRE	O	IDE_DIOR		O	NF_NRE	O
CF_D0	B	IDE_D0	CF_D0	B	-	-
CF_D1	B	IDE_D1	CF_D1	B	-	-
CF_D2	B	IDE_D2	CF_D2	B	-	-
CF_D3	B	IDE_D3	CF_D3	B	-	-
CF_D4	B	IDE_D4	CF_D4	B	-	-
CF_D5	B	IDE_D5	CF_D5	B	-	-
CF_D6	B	IDE_D6	CF_D6	B	-	-
CF_D7	B	IDE_D7	CF_D7	B	-	-
CF_D8	B	IDE_D8	CF_D8	B	-	-
CF_D9	B	IDE_D9	CF_D9	B	-	-
CF_D10	B	IDE_D10	CF_D10	B	-	-
CF_D11	B	IDE_D11	CF_D11	B	-	-
CF_D12	B	IDE_D12	CF_D12	B	-	-
CF_D13	B	IDE_D13	CF_D13	B	-	-
CF_D14	B	IDE_D14	CF_D14	B	-	-
CF_D15	B	IDE_D15	CF_D15	B	-	-

*1: It is a register, which can be set by firmware.

6. AC Characteristics

6.1 Serial Peripheral Interface

- SPI mode 0

Symbol	Parameter	Min.	Max.	Unit
tClSh	-CS low to SCK high	-	230	ns
tShCh	SCK high to –CS high	-	125	ns
tCRT	Clock Rise Time	0.1	-	V/ns
tCFT	Clock Fall Time	0.1	-	V/ns
tSU:DAT	Data in Setup Time	10	-	ns
tHD:DAT	Data in Hold Time	5	-	ns
tV	Output Valid	-	5	ns
tHO	Output Hold Time	-	5	ns
tWH	SCK High Time	-	35	ns
tWL	SCK Low Time	-	35	ns

* The definition of signal timing is defined by SPI_SCK=13.5MHz.

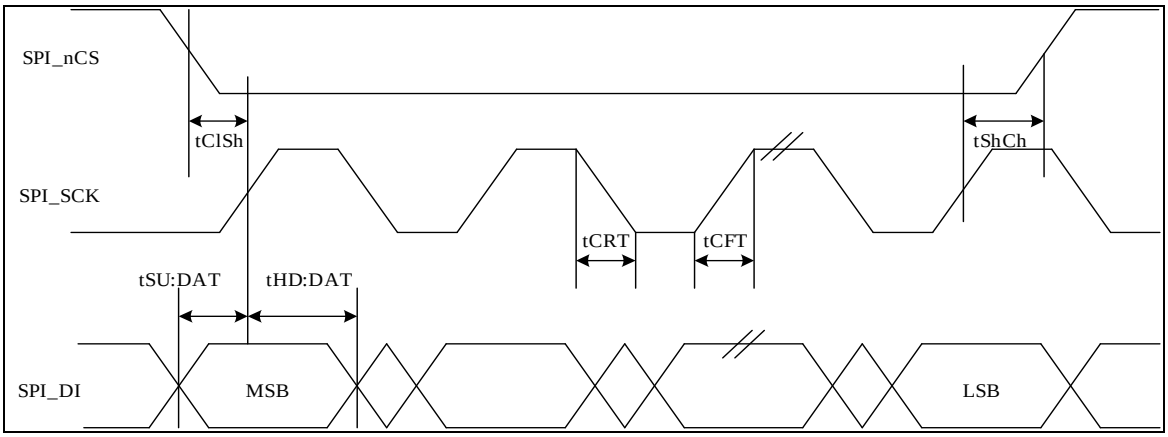


Figure 6.1: Input Timing Diagram of SPI

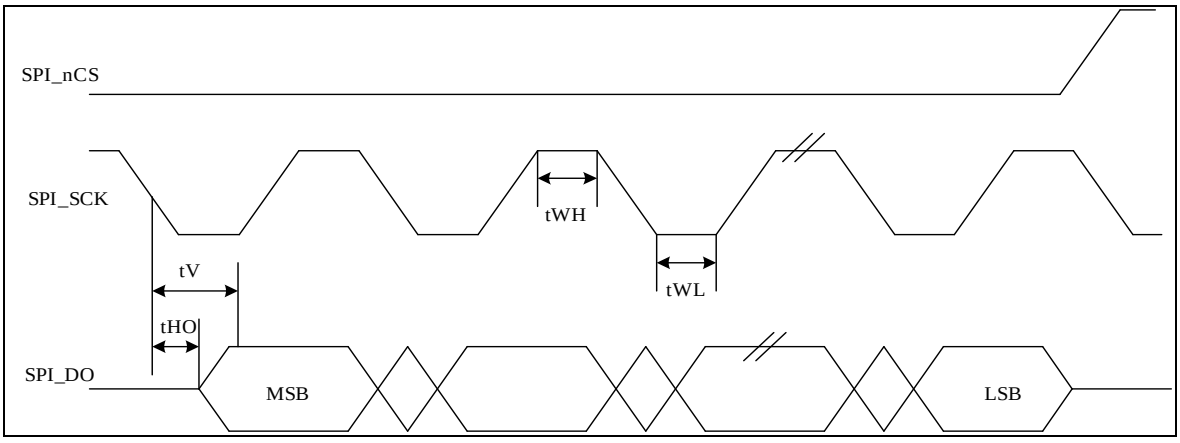


Figure 6.2: Output Timing Diagram of SPI

6.2 Inter-IC Sound Interface

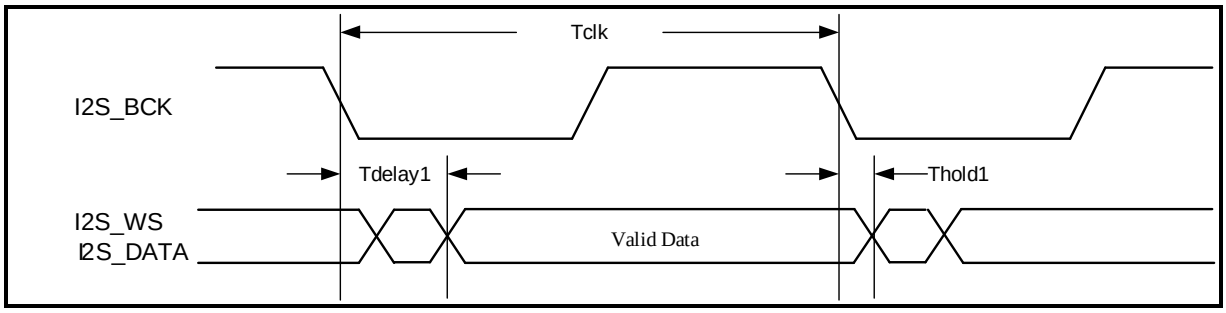


Figure 6.3: Timing Diagram of I2S

Symbol	Parameter	Min.	Max.	Unit
Tclk	Bit clock frequency	20.84	125	us
Tdelay1	output delay from CLK rising edge	0	3	ns
Thold1	output data hold time from CLK rising edge	0	3	ns

6.3 I2C Interface

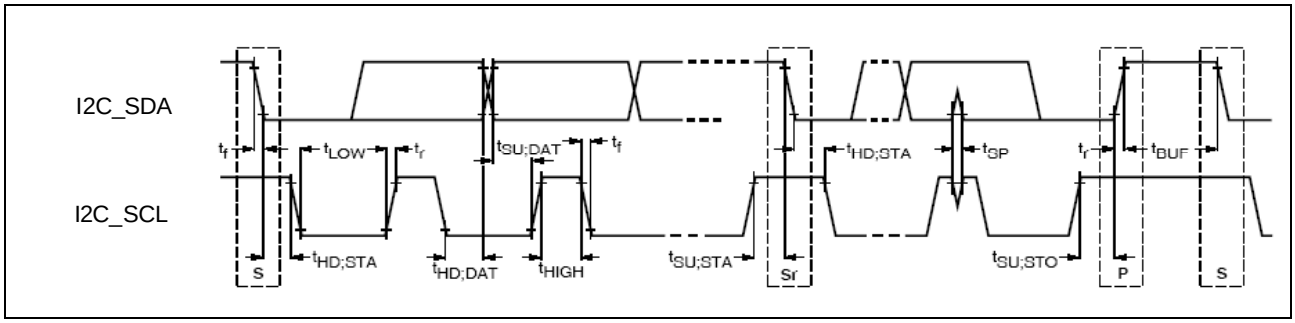


Figure 6.4: Timing Diagram of I2C-bus

Symbol	Parameter	Standard-Mode		Fast- Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	KHz
$t_{HD;\ STA}$	Hold time (repeated) START condition After this period, the first clock pulse is generated	4.0	-	0.6	-	us
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	us
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	us
$t_{SU;\ STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	us
$t_{HD;\ DAT}$	Data hold time for I2C bus devices	0	3.45	0	0.9	us
$t_{SU;\ DAT}$	Data set-up time	250	-	100	-	ns
t_r	Rise time of both SDA and SCL signals	-	1000	$20+0.1C_b$	300	ns
t_f	Fall time of both SDA and SCL signals	-	300	$20+0.1C_b$	300	ns
$t_{SU;\ DAT}$	Set-up time for STOP condition	4.0	-	0.6	-	us
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	us
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes

1. C_b = total capacitance of one bus line in PF.
2. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

6.4 SDRAM Interface

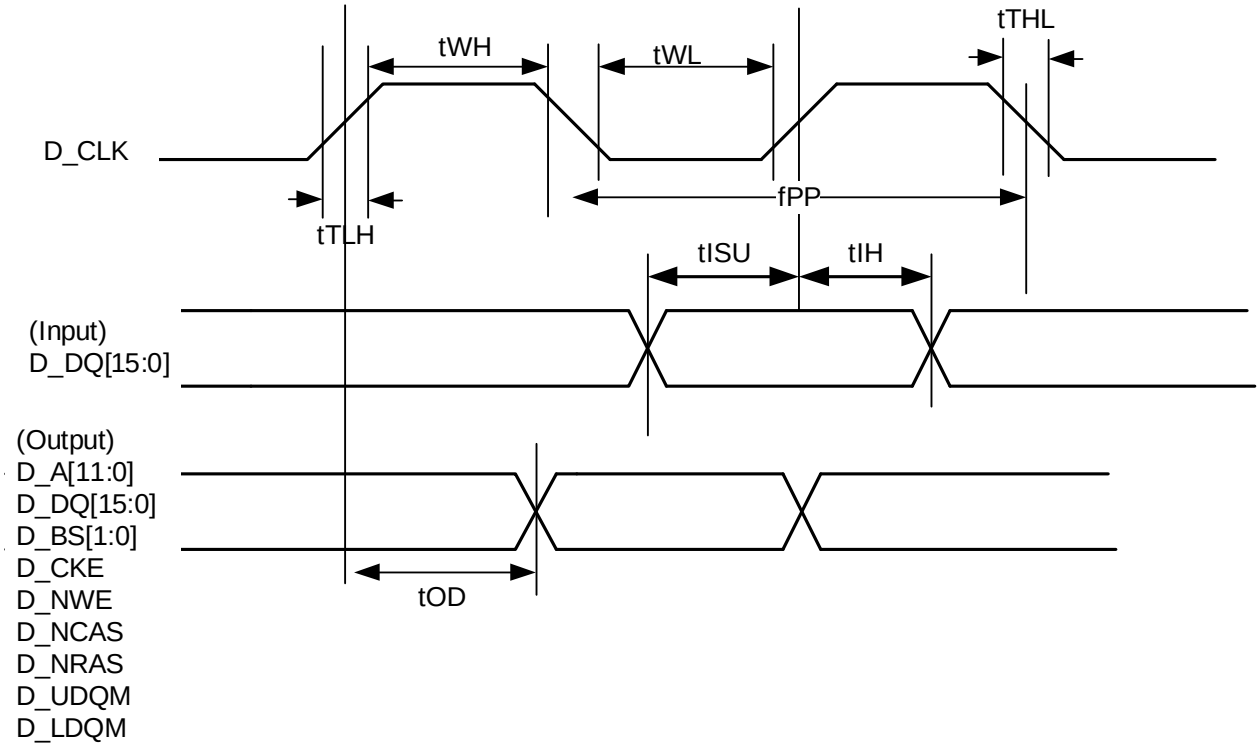


Figure 6.5: Timing Diagram of SDRAM Interface

Symbol	Parameter	Min.	Max.	Unit
fPP	Clock frequency	-	108	MHz
tWL	Clock low time	4.62	-	ns
tWH	Clock High time	4.62	-	ns
tTLH	Clock rise time		2	ns
tTHL	Cock fall time		2	ns
tISU	Input set-up time	2		ns
tIH	Input hold time	1		ns
tOD	Output delay time		3.5	ns

6.5 Secure Digital/ MultiMedia Card Interface

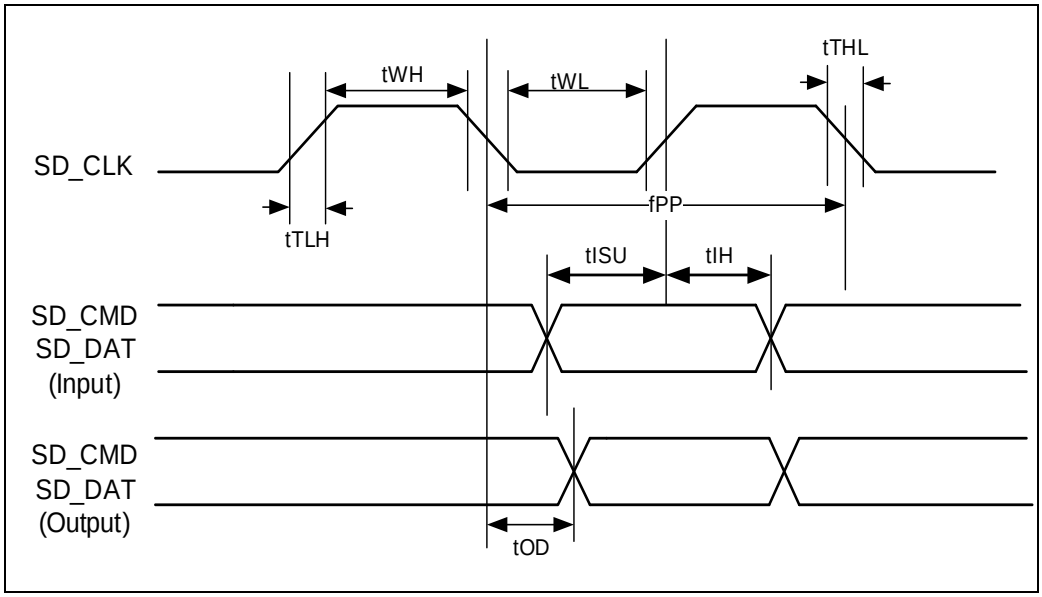


Figure 6.11: Timing Diagram of Data Input/Output Referenced to Clock

Symbol	Parameter	Min.	Max.	Unit
fPP	Clock frequency	-	36	MHz
tWL	Clock low time	20	-	ns
tWH	Clock High time	7	-	ns
tTLH	Clock rise time		3	ns
tTHL	Cock fall time		3	ns
tISU	Input setup time	10		ns
tIH	Input hold time	5		ns
tOD	Output delay time		3	ns

* The definition of signal timing is defined by SD_CLK=36MHz.

6.6 XD / NAND Flash Interface

Symbol	Parameter	Min.	Max.	Unit
tCLhWl	CLE high to –WE low	27	-	ns
tWhCLl	-WE high to CLE low	55	-	ns
tClWl	-CE low to –WE low	27	-	ns
tWhCh	-WE high to –CE high	55	-	ns
tWP	-WE pulse width	55	-	ns
tALhWl	ALE high to –WE low	27	-	ns
tWhALl	-WE high to ALE low	80	-	ns
tDS	Data setup time	10	-	ns
tDH	Data hold time	5	-	ns
tWC	Write cycle time	135	-	ns
tWH	-WE high hold time	80	-	ns
tRR	Ready to –RE Low	70	-	ns
tRP	Read pulse width	55	-	ns
tRC	Read cycle time	135	-	ns
tOD	-WE output delay time	-	0	ns
tREH	-RE high hold time	80	-	ns

* The definition of signal timing is defined by Peri_clk=36MHz.

* The definition of read/write pulse width is defined with 2*Peri_clk, this timing can be redefined by setting register.

* The definition of read/write high hold time is defined with 3*Peri_clk, this timing can be redefined by setting register.

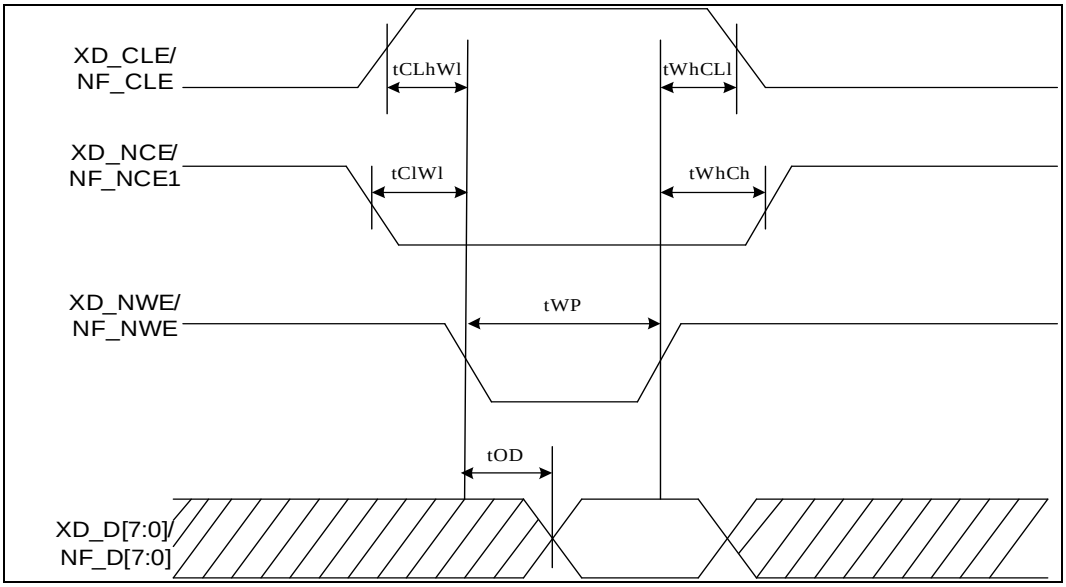


Figure 6.12: Command output Timing

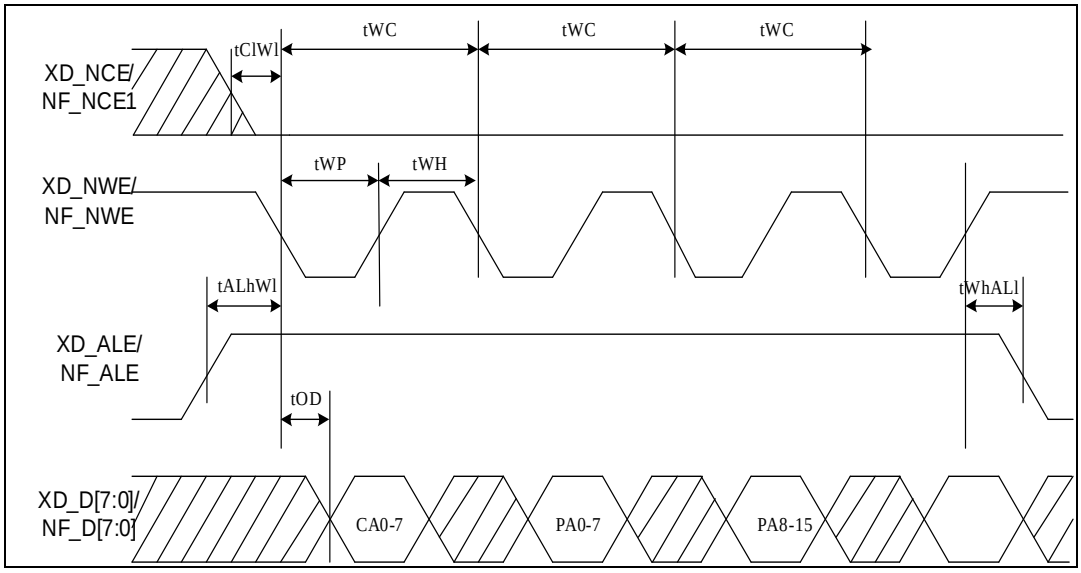


Figure 6.13: Address output Timing

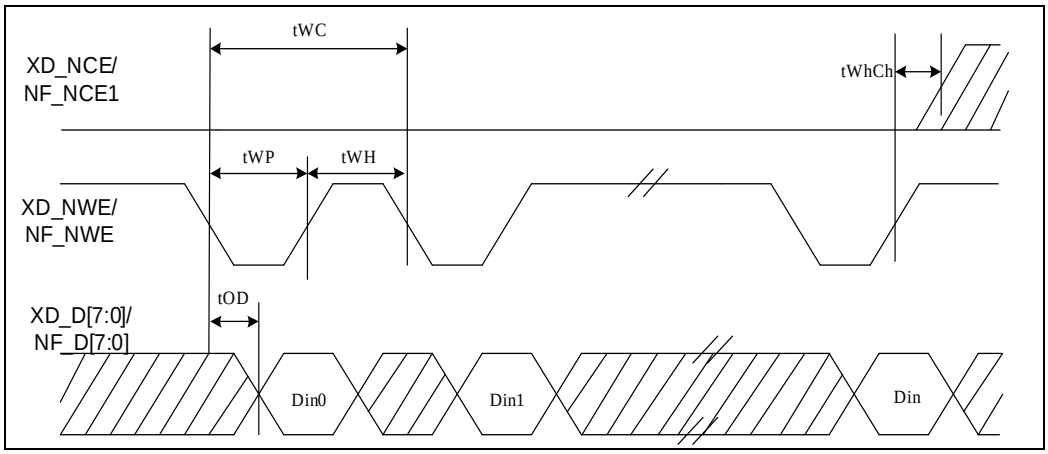


Figure 6.14: Data output Timing

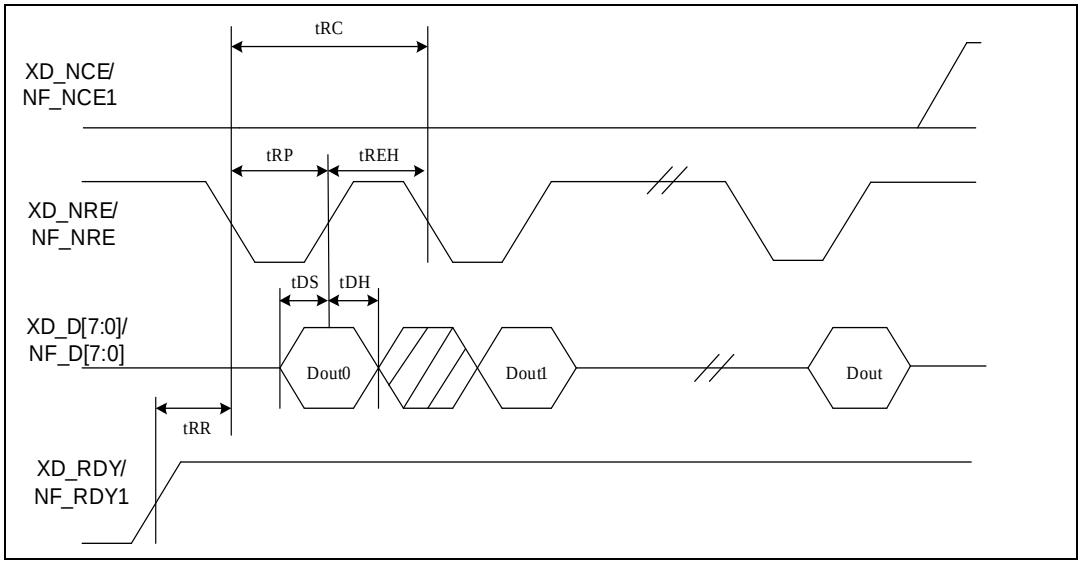


Figure 6.15: Data Input Timing

6.7 CompactFlash Card /ATA Interface

- **True IDE PIO Mode Read/Write Timing Specification**

Name	Item	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Note
to	Cycle time(min)	600	383	240	180	120	100	80	
t1	Address Valid to CF_DIOR /CF_DIOW setup(min)	70	50	30	30	25	15	10	
t2	CF_DIOR/CF_DIOR (min)	165	125	100	80	70	65	55	
t2	CF_DIOR/CF_DIOR Register	290	290	290	80	70	65	55	
t2i	CF_DIOR/CF_DIOR Recovery time(min)	-	-	-	70	25	25	20	
t3	CF_DIOW data setup (min)	60	45	30	30	20	20	15	
t4	CF_DIOW data hold (min)	30	20	15	10	10	5	5	
t5	CF_DIOR data setup (min)	50	35	20	20	20	15	10	

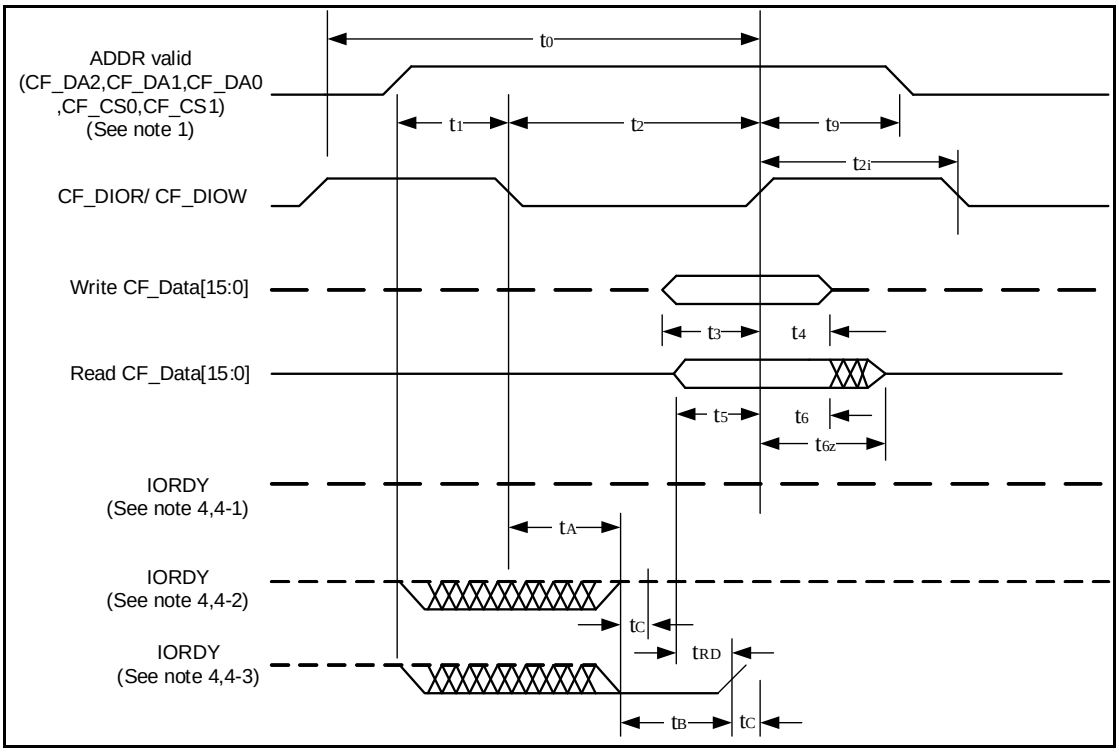


Figure 6.16: Timing Diagram of True IDE PIO Mode

Notes:

(1) Device address consists of CF_CS0, CF_CS1, and CF_DA [2:0]

(2) Data consists of CF_Data[15:00] (16-bit)

(3) The negation of CF_IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of CF_DIOR or CF_DIOW. The assertion and negation of CF_IORDY is described in the following three cases:

(4-1) Device never negates CF_IORDY: No wait is generated.

(4-2) Device starts to drive CF_IORDY low before tA, but causes CF_IORDY to be asserted before tA: No wait generated.

(4-3) Device drives CF_IORDY low before tA: wait generated. The cycle completes after CF_IORDY is reasserted. For cycles where a wait is generated and CF_IORDY is asserted, the device shall place read data on CF_Data[15:00] for tRD before causing CF_IORDY to be asserted.

- **True IDE Multiword DMA Mode Read/Write Timing Specification**

Name	Item	Mode0 (ns)	Mode1 (ns)	Mode2 (ns)	Mode3 (ns)	Mode4 (ns)
t_O	Cycle time(min)	480	150	120	100	80
t_D	CF_DIOR/CF_DIOW asserted width(min)	215	80	70	65	55
t_E	CF_DIOR data access(max)	150	60	50	50	45
t_F	CF_DIOR data hole(min)	5	5	5	5	5
t_G	CF_DIOR/CF_DIOW data setup(min)	100	30	20	15	10
t_H	CF_DIOW data hold(min)	20	15	10	5	5
t_I	CF_DMACK to CF_DIOR/CF_DIOW setup(min)	0	0	0	0	0
t_J	CF_DIOR/CF_DIOW to CF_DMACK hold(min)	20	5	5	5	5
t_{KR}	CF_DIOR negated width(min)	50	50	25	25	20
t_{KW}	CF_DIOW negated width(min)	215	50	25	25	20
t_{LR}	CF_DIOR to CF_DMARQ delay(max)	120	40	35	35	35
t_{LW}	CF_DIOW to CF_DMARQ delay(max)	40	40	35	35	35
t_M	CF_CS(1:0)valid to CF_DIOR/CF_DIOW	50	30	25	10	5
t_N	CF_CS(1:0) hold	15	10	10	10	10
t_Z	CF_DMACK	20	25	25	25	25

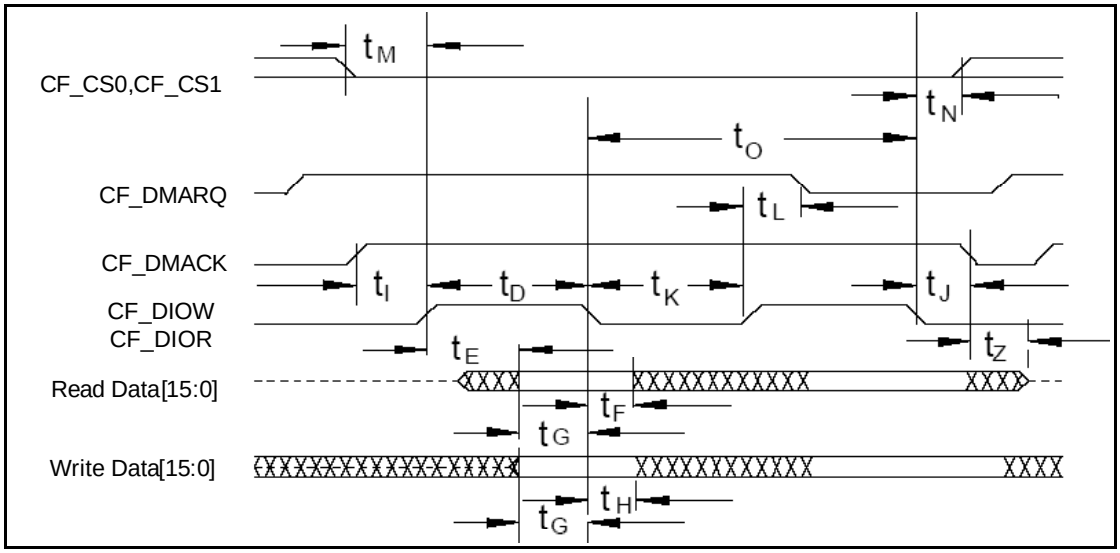


Figure 6.17: Timing Diagram of True IDE Multiword DMA Mode Read/Write

- **True IDE Ultra DMA Mode Read/Write Timing Specification**

Signal	Alias name for Ultra DMA Mode	Note
CF_DIOR	HDMARDY or HSTROBE	
CF_DIOW	STOP	
CF_IORDY	DDMARDY or DSTROBE	

Name	UDMA Mode0 (ns)		UDMA Mode1 (ns)		UDMA Mode2 (ns)		UDMA Mode3 (ns)		UDMA Mode4 (ns)		Measurement Location
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		Sender
t_{CYC}	112		73		54		39		25		
t_{2CYC}	230		153		115		86		57		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		Host
t_{ZFS}	0		0		0		0		0		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{FS}		230		200		170		130		120	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	
t_{MLI}	20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10	
t_{ZAH}	20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Host
t_{RFS}		75		70		60		60		60	Sender
t_{RP}	160		125		100		100		100		Recipient
t_{IORDYZ}		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		Device

t_{ACK}	20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		Sender

Name	Comment	Note
t_{2CYTYP}	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	
t_{CS}	CRC word setup time at device	
t_{CH}	CRC word hold time device	
t_{CVS}	CRC word valid setup time at host (from CRC valid until –DMACK negation)	
t_{CVH}	CRC word valid hold time at sender (from –DMACK negation until CRC may become invalid)	
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	
t_{MLI}	Interlock time with minimum	
t_{UI}	Unlimited interlock time	
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	Drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from –DMACK so STOP and –HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of –DMARDY)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after	

Name	Comment	Note
t_{2CYTYP}	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	
	negating –DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	
t_{ZIORDY}	Minimum time before driving IORDY	
t_{ACK}	Setup and hold times for –DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

- **Initial an Ultra DMA Data-In Burst**

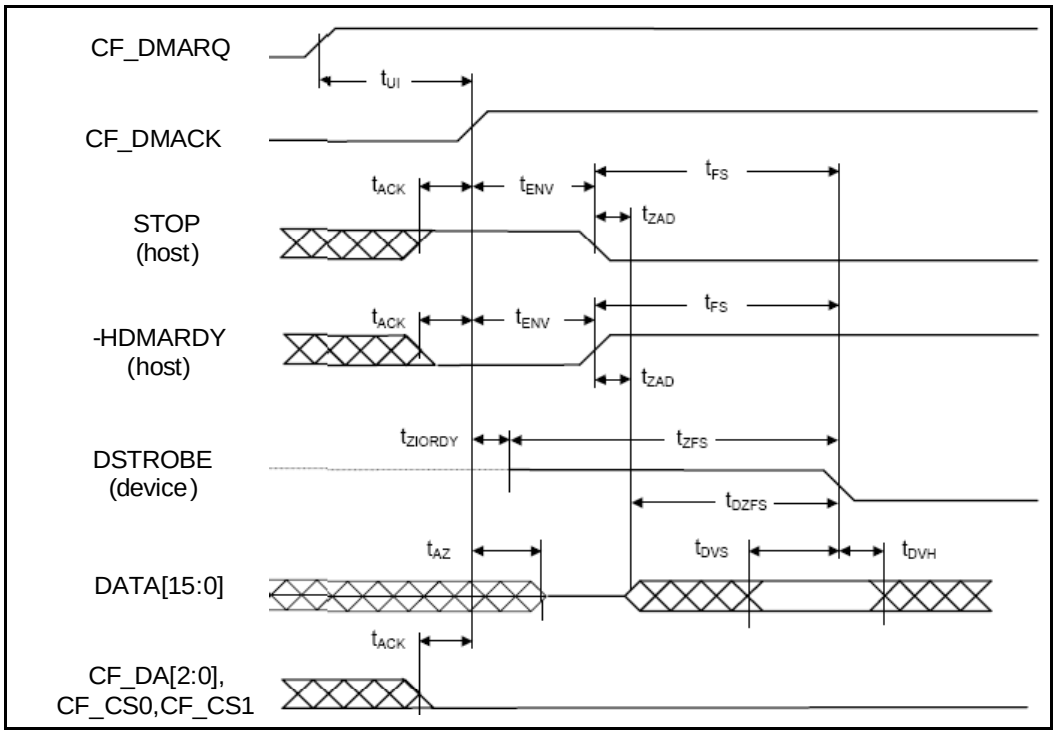


Figure 6.18: Initiation Timing Diagram of Ultra DMA Data-In Burst

- **Sustaining an Ultra DMA Data-In Burst**

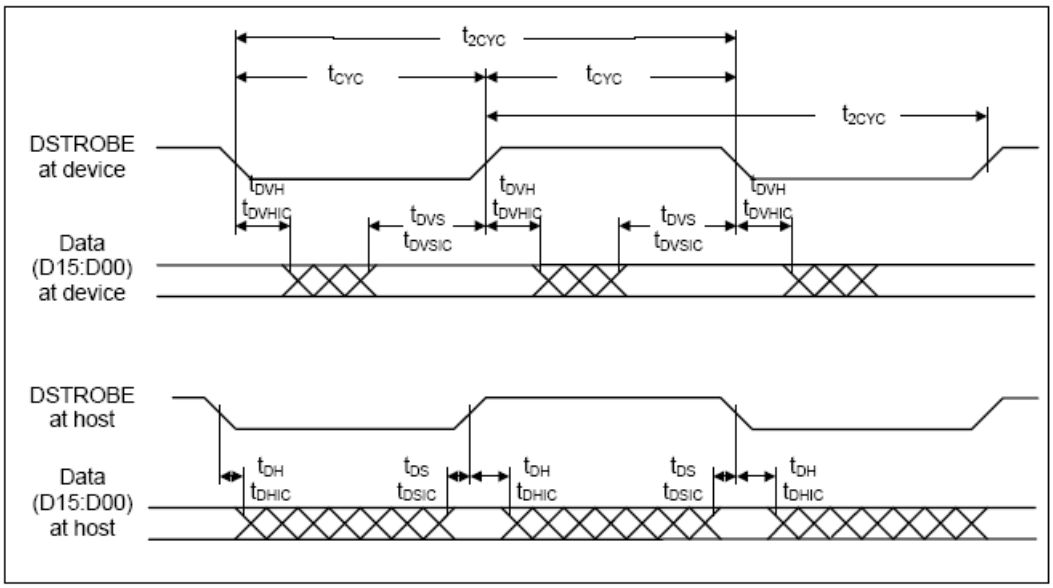
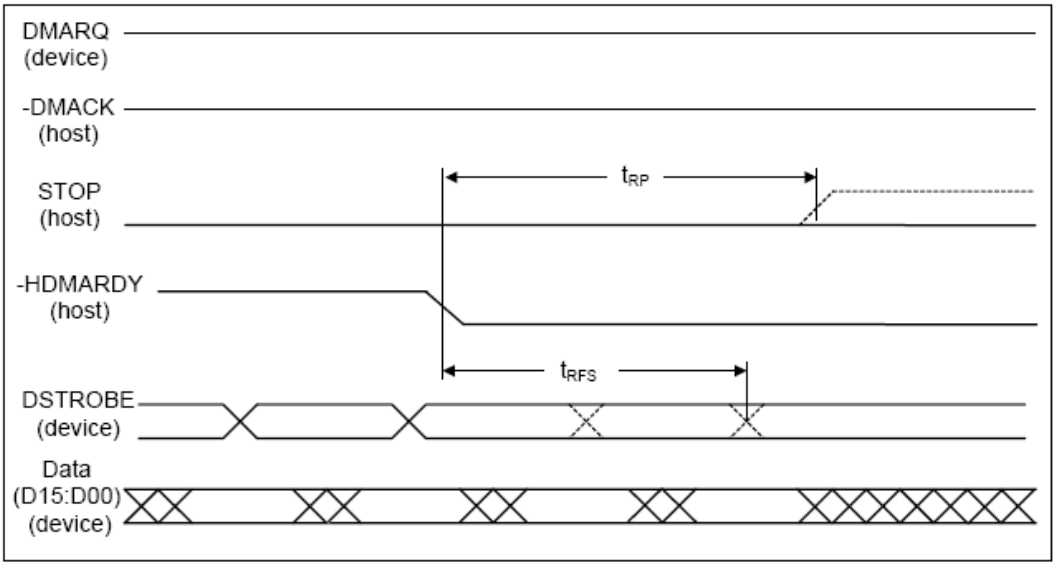


Figure 6.19: Sustained Ultra DMA Data-In Burst Timing Diagram

- **Host Pausing an Ultra DMA Data-In Burst**



Notes: 1) The host may assert STOP to request termination of the Ultra DMA burst no sooner than t_{RP} after -HDMARDY is negated.

2) After negating -HDMARDY, the host may receive zero, one, two, or three more data words from the device.

Figure 6.20: Ultra DMA Data-In Burst Host Pause Timing Diagram

- **Device Terminating an Ultra Data-In Burst**

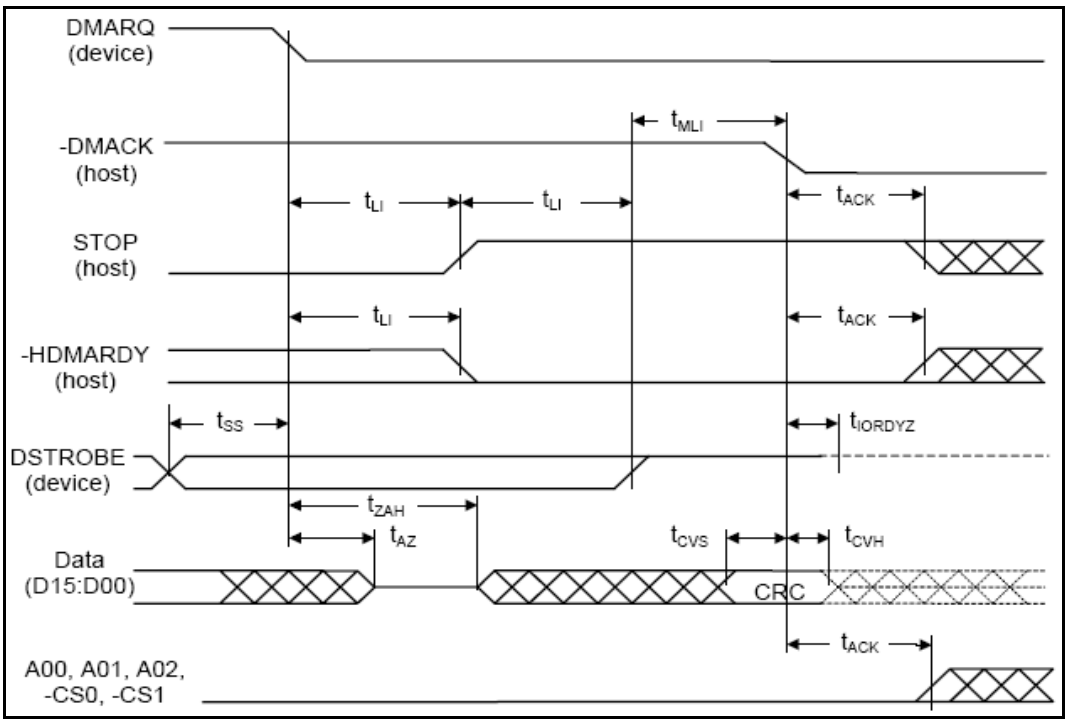


Figure 6.21: Ultra DMA Data-In Burst Device Termination Timing Diagram

- **Host Terminating an Ultra DMA Data-In Burst**

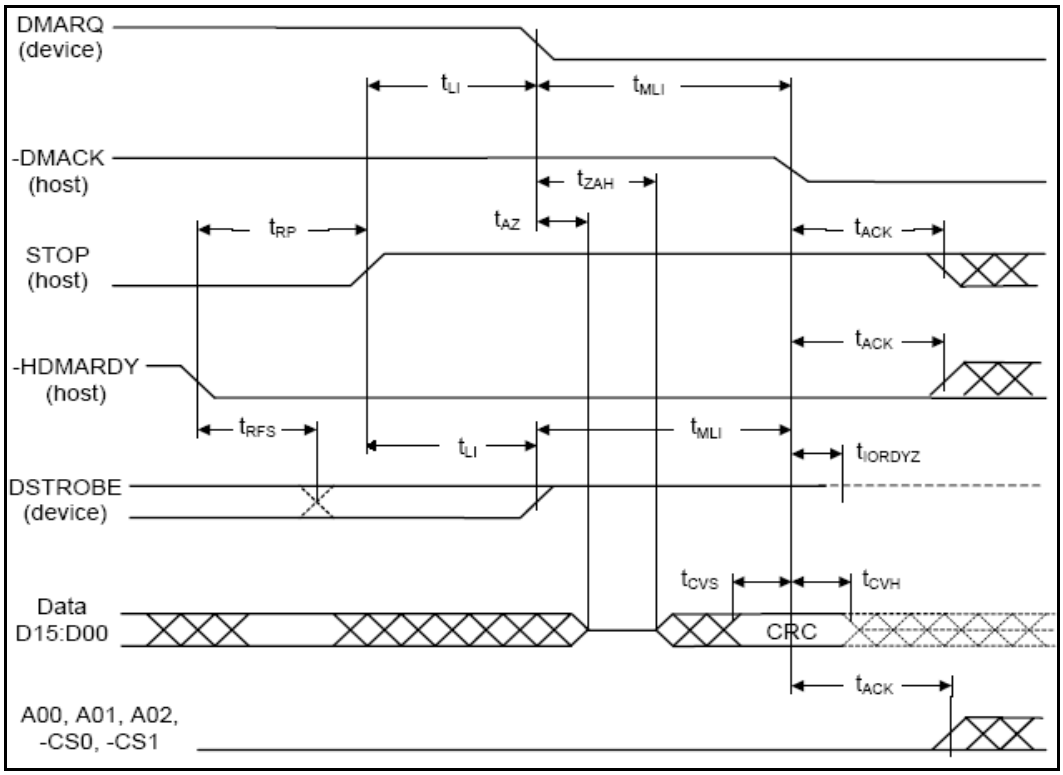


Figure 6.22: Ultra DMA Data-In Burst Host Termination Timing Diagram

- **Initial an Ultra DMA Data-Out Burst**

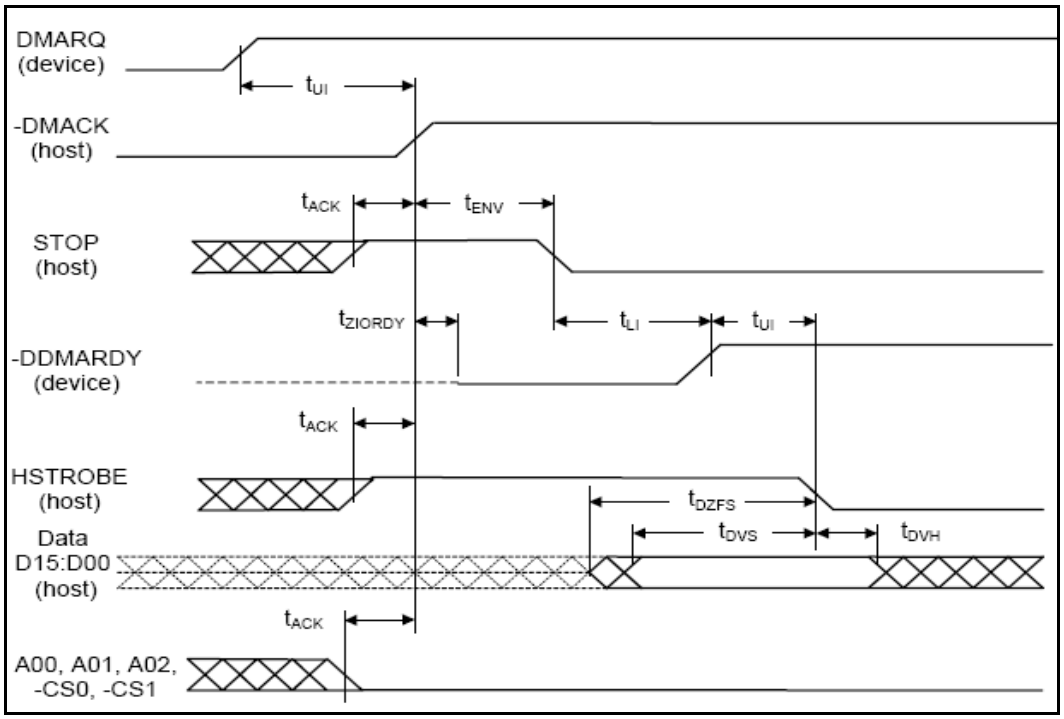


Figure 6.23: Ultra DMA Data-Out Burst Initiation Timing Diagram

- **Sustaining an Ultra DMA Data-out Burst**

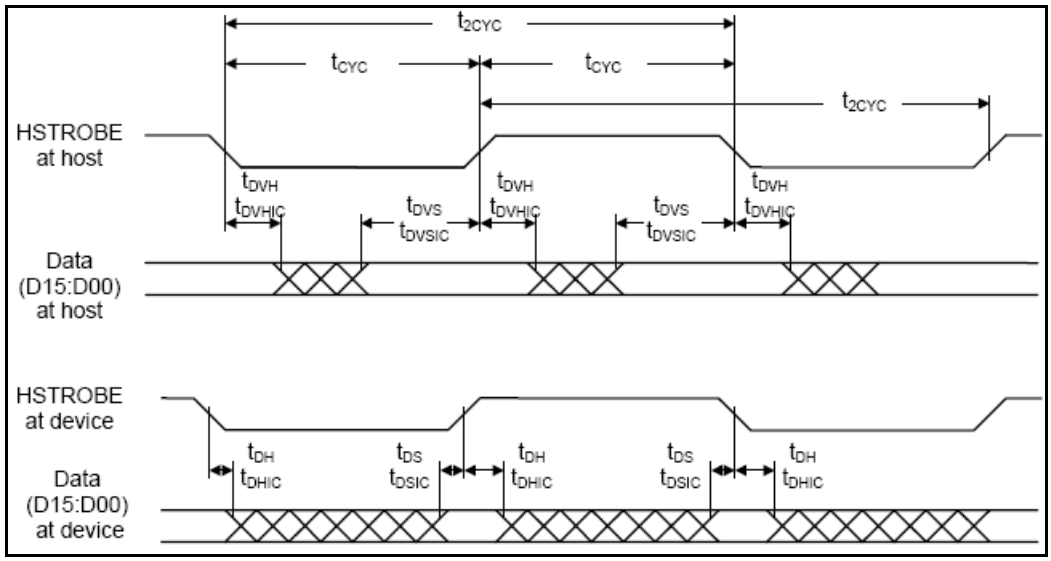


Figure 6.24: Sustained Ultra DMA Data-Out Burst Timing Diagram

- **Device Pausing an Ultra DMA Data-Out Burst**

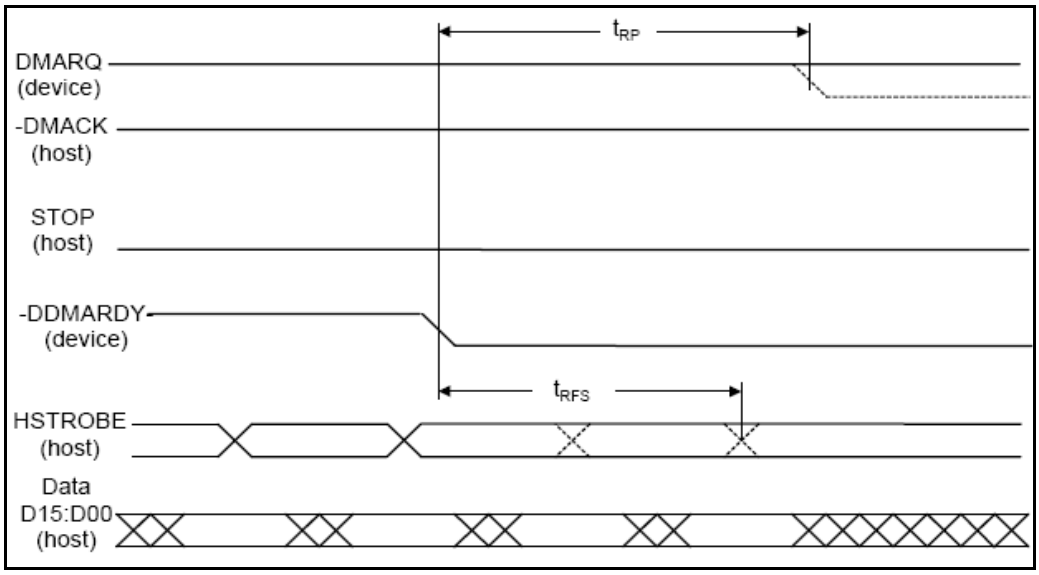


Figure 6.25: Ultra DMA Data-Out Burst Device Pause Timing Diagram

- **Device Terminating an Ultra DMA Data-Out Burst**

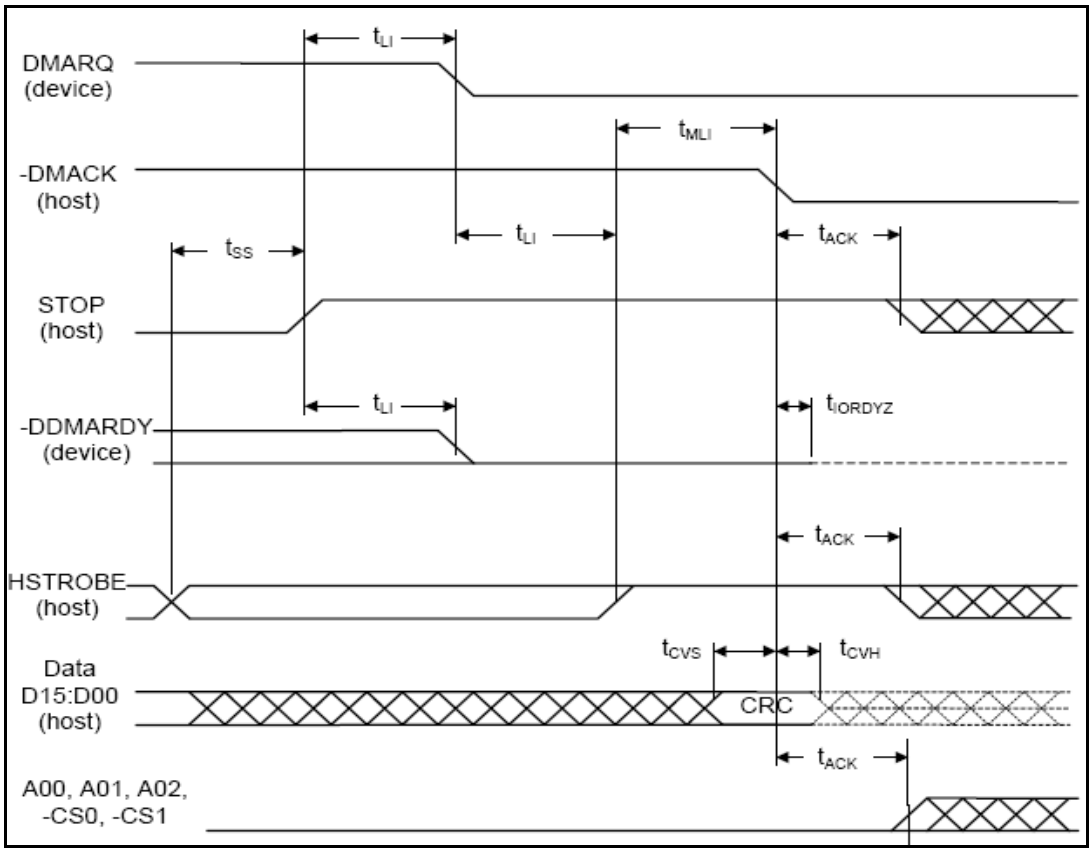


Figure 6.26: Ultra DMA Data-Out Burst Device Termination Timing Diagram

6.8 Digital Display Interface

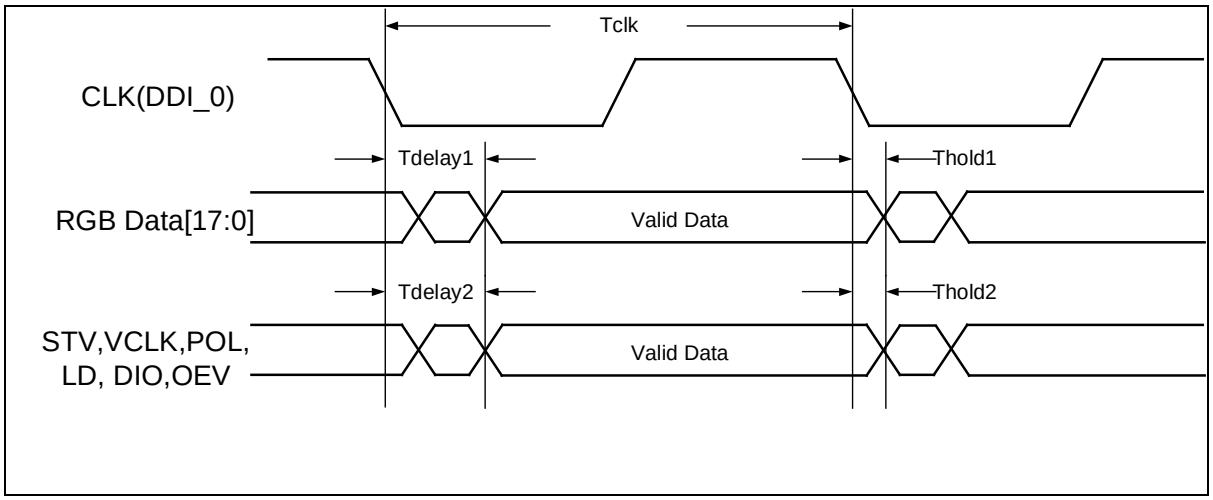


Figure 6.27: Timing Diagram of Digital Display Interface

Symbol	Parameter	Min.	Max.	Unit
Fclk	Pixel clock frequency (Fclk = 1/Tclk)	25	32	MHz
Tdelay1	RGB Data output delay from CLK rising edge	0	5	ns
Thold1	RGB Data output data hold time from CLK rising edge	0	5	ns
Tdelay2	STV, VCLK, POL, LD, DIO, OEV output delay from CLK rising edge	0	3	ns
Thold2	STV, VCLK, POL, LD, DIO, OEV output data hold time from CLK rising edge	0	3	ns

7. Electrical Characteristic

- Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD33 AVDD33_VID AVDD33_AUD USB_AVDD33_BIAS USB_AVDD33_TRV	Power Supply (3.3V)	-0.3 to 3.6	V
VDD18 AVDD18_PLL AVDD18_VID USB_AVDD18_PLL USB_AVDD18_CDR	Power Supply (1.8V)	-0.3 to 1.98	V
V_{IN}	Input Voltage	-0.3 to V_{CC}+0.3	V
V_{OUT}	Output Voltage	-0.3 to V_{CC}+0.3	V
T_{STG}	Storage Temperature	-55 to 150	℃

- Recommended Operation Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD33/AVDD33_VID/AVDD33_AUD/USB_AVDD33_BIAS/ USB_AVDD33_TRV	Power Supply (3.3V)	3.0	3.3	3.6	V
VDD18/AVDD18_PLL/AVDD18_VID/ USB_AVDD18_PLL/USB_AVDD18_CDR	Power Supply (1.8V)	1.62	1.8	1.98	V
T_{OPR}	Operating Temperature	0	25	70	℃

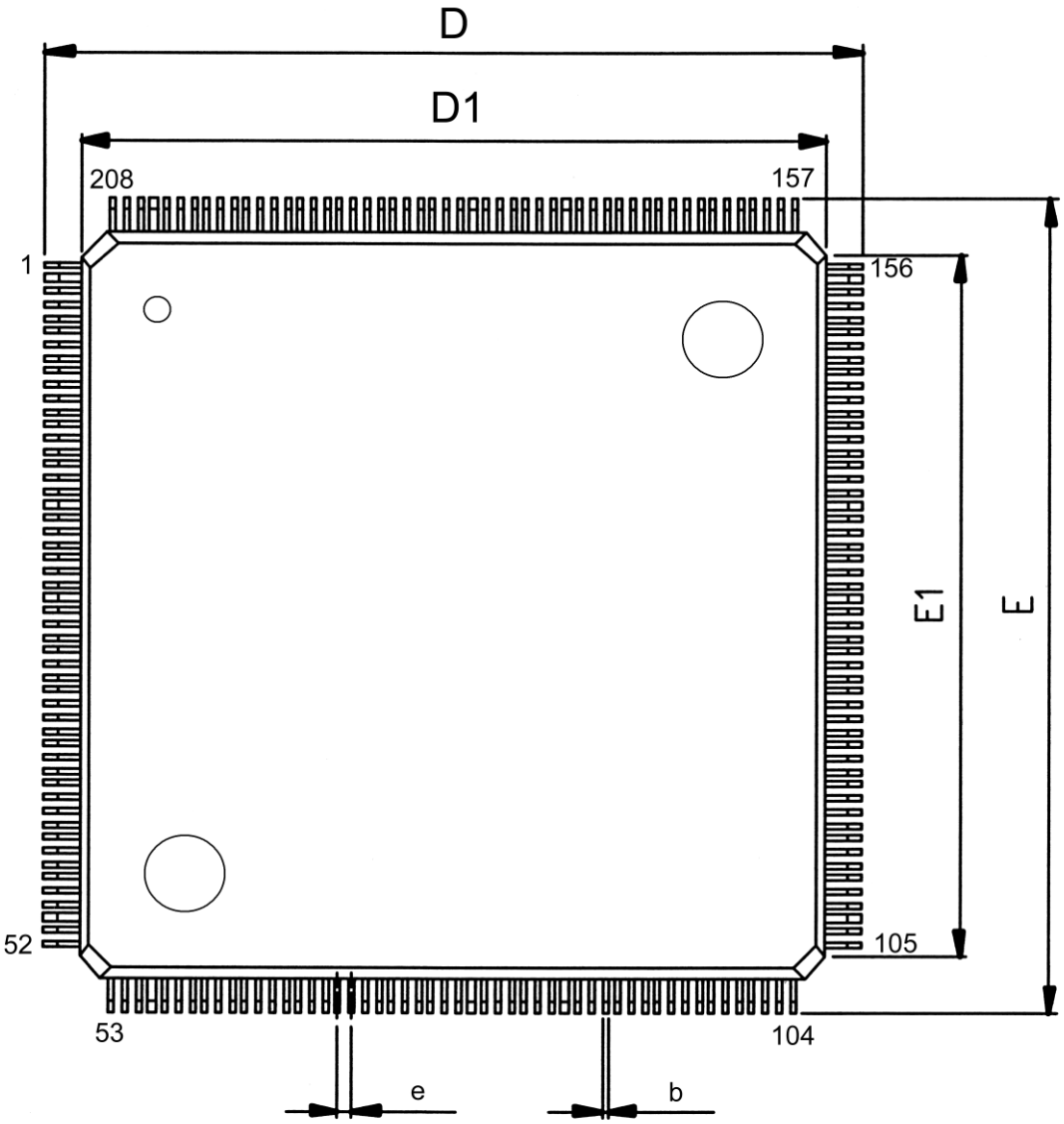
- DC Electrical Characteristics for 3.3 volts operation

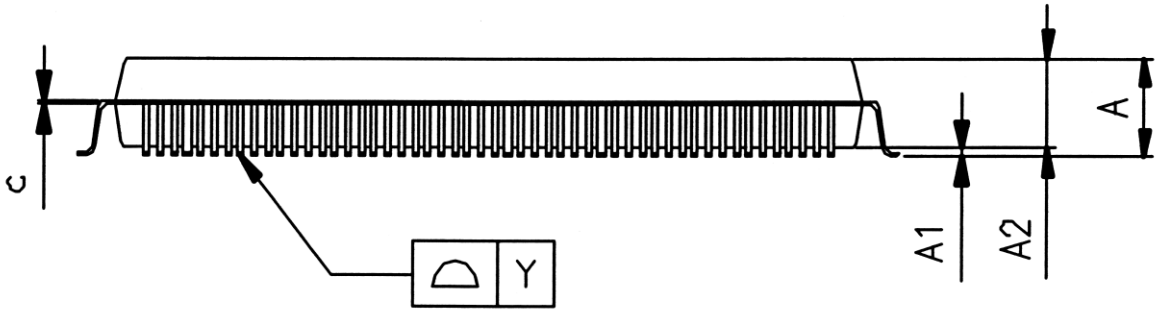
(Under Recommended Operating Conditions and V_{CC} = 3.0V ~ 3.6V, Tj = 0℃ to + 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	-0.3		0.8	V
V_{IH}	Input High Voltage	2.0		Vcc+0.3	V
V_{T-}	Schmitt Input Low Voltage	-0.3		0.8	V
V_{T+}	Schmitt Input High Voltage	2.0		Vcc+0.3	V
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	2.4			V

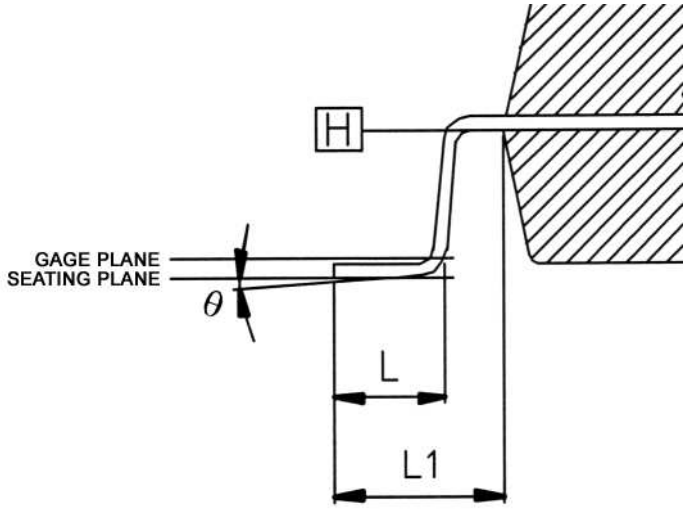
8. Package Outline and Dimension

- Package Outline (208-pin PQFP)





- Package Outline (208-pin PQFP) – continued



- Dimension (208-pin PQFP)

Dimension	Min	Nom	Max
A	-	-	4.10
A1	0.25	-	0.50
A2	3.20	3.40	3.60
b	0.17	-	0.27
c	0.11	-	0.23
D	31.20 BSC		
D1	28.00 BSC		
E	31.20 BSC		
E1	28.00 BSC		
e		0.50 BSC	
L	0.73	0.88	1.03
L1		1.60 REF	
Y	-	-	0.08
θ	0°	-	8°

Unit: mm

REF: Reference

BSC: Basic Spacing between Centers (integrated circuit package dimension)

9. Chip Revision History

Revision	Description of Changes	Date
JL4203A	First Announce	2007/3/20
JL4209A	● Correct core voltage to 1.8 volts. ● Fix some bugs in MP3 block. ● Modify the function of internal pattern generator to control backlight brightness of LCD panel via GPIO_33 (pin 90). ● Improve the performance of AVI playback on digital panel. ● Speed up transient effect of photo playback on digital panel.	2007/9/10

10. Ordering Information

Part Number	Package	Status	Note
JL4209A-V2	208-pin PQFP	Available	N/C

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