

Dual N-Channel 20-V (D-S) MOSFET

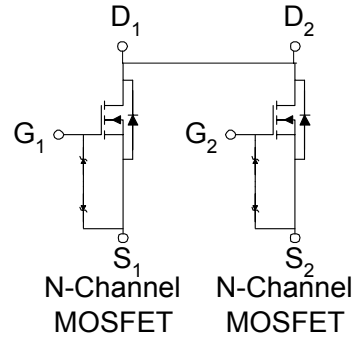
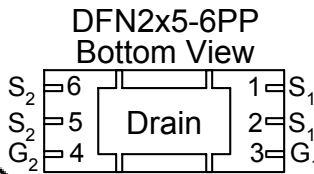
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
20	22 @ $V_{GS} = 4.5V$	11
	28 @ $V_{GS} = 2.5V$	9.2

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN2x5-6PP saves board space
- Fast switching speed
- High performance trench technology



ESD Protected
2000V



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current ^a	$T_A = 25^\circ C$	I_D	11	A
	$T_A = 70^\circ C$		8.5	
Pulsed Drain Current ^b		I_{DM}	± 40	
Continuous Source Current (Diode Conduction) ^a		I_S	3.1	A
Power Dissipation ^a	$T_A = 25^\circ C$	P_D	3.5	W
	$T_A = 70^\circ C$		1.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	$R_{\theta JA}$	36	$^\circ C/W$
	Steady State		76	$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	0.5			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 10	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			30	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	20			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 4.5 \text{ V}, I_D = 0.5 \text{ A}$			22	m Ω
		$V_{GS} = 2.5 \text{ V}, I_D = 0.5 \text{ A}$			28	
Forward Transconductance ^A	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 6 \text{ A}$		22		S
Diode Forward Voltage	V_{SD}	$I_S = 0.5 \text{ A}, V_{GS} = 0 \text{ V}$		0.7		V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_D = 6 \text{ A}$		9.2		nC
Gate-Source Charge	Q_{gs}			1.9		
Gate-Drain Charge	Q_{gd}			2.8		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10 \text{ V}, R_L = 15 \Omega, I_D = 1 \text{ A},$ $V_{GEN} = 4.5 \text{ V}$		1.7		nS
Rise Time	t_r			2.3		
Turn-Off Delay Time	$t_{d(off)}$			1.1		
Fall-Time	t_f			4.4		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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