SONY

Distribution Restraint	Internal	Outside
	Approved	Approved

SP10T Antenna Switch Module for 6TRx/2Tx/2Rx with SPI I/F

CXM3588UR

Description

The CXM3588UR is a SP10T antenna switch module for GSM/UMTS/CDMA/LTE multi-mode handset
The CXM3588UR has a built-in dual low pass filter and a +1.8 V CMOS compatible decoder with SPI function.

The Sony GaAs junction gate pHEMT (JPHEMT) MMIC process is used for low insertion loss and high linearity.
The device has low BOM with no DC blocking Capacitor.

Features

- ◆Low Insertion Loss: 0.50 dB (Typ.) TRx (Cellular Band)
  0.70 dB (Typ.) TRx (IMT Tx Band)
- ◆High Linearity: IIP3=68 dBm
- ◆Low Voltage Operation: Vdd=2.5 V
- ◆Supports CMOS control for serial interface
- ◆No DC Blocking Capacitors except sourcing DC bias
- ◆Small Package Size: UQFN-26P (2.6 mm x 3.4 mm x 0.625 mm Max.)
- ◆Lead-Free and RoHS Compliant

Structure

GaAs Junction Gate pHEMT (JPHEMT) MMIC Switch, CMOS Decoder

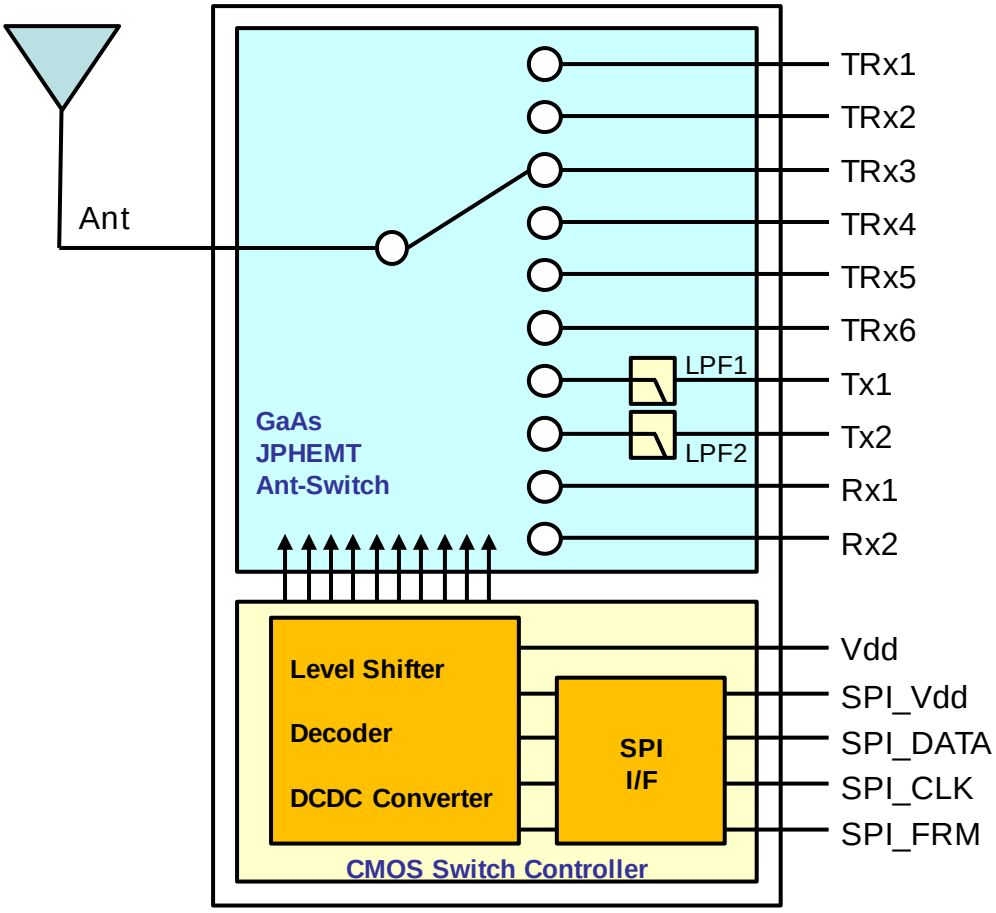
Absolute Maximum Ratings

◆Bias Voltage	Vdd	4 V (Ta = 25 °C)
◆Supply Voltage for SI	SPI_Vdd	3.6 V (Ta=25 °C)
◆Control Voltage for SI	SPI_CLK, FRM, DATA	3.6 V (Ta = 25 °C)
◆Maximum input power	[Tx1]	36 dBm (Duty cycle = 12.5% to 50%) (Ta = 25 °C)
	[Tx2]	34 dBm (Duty cycle = 12.5% to 50%) (Ta = 25 °C)
	[TRx]	32 dBm (Ta = 25 °C)
	[Rx]	13 dBm (Ta = 25 °C)
◆Operating Temperature		-35 °C to +90 °C
◆Storage Temperature		-65 °C to +150 °C

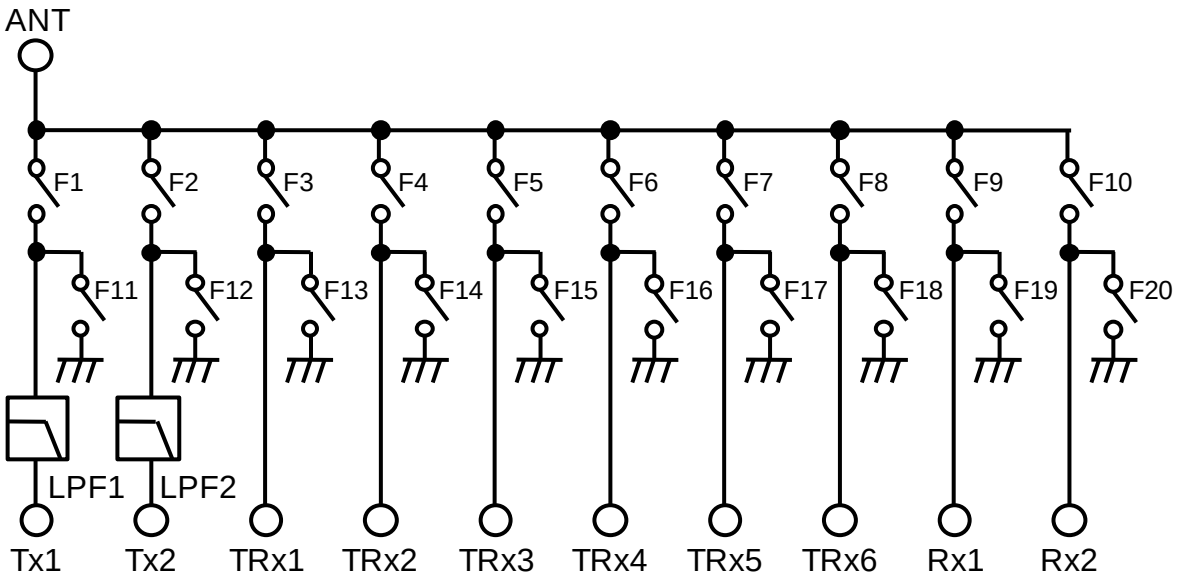
This IC is ESD sensitive device. Special handling precautions are required.

E12310B29

Block Diagram of SP10T Antenna Switch Module with SPI



Block Diagram of SP10T 6TRx/2Tx/2Rx



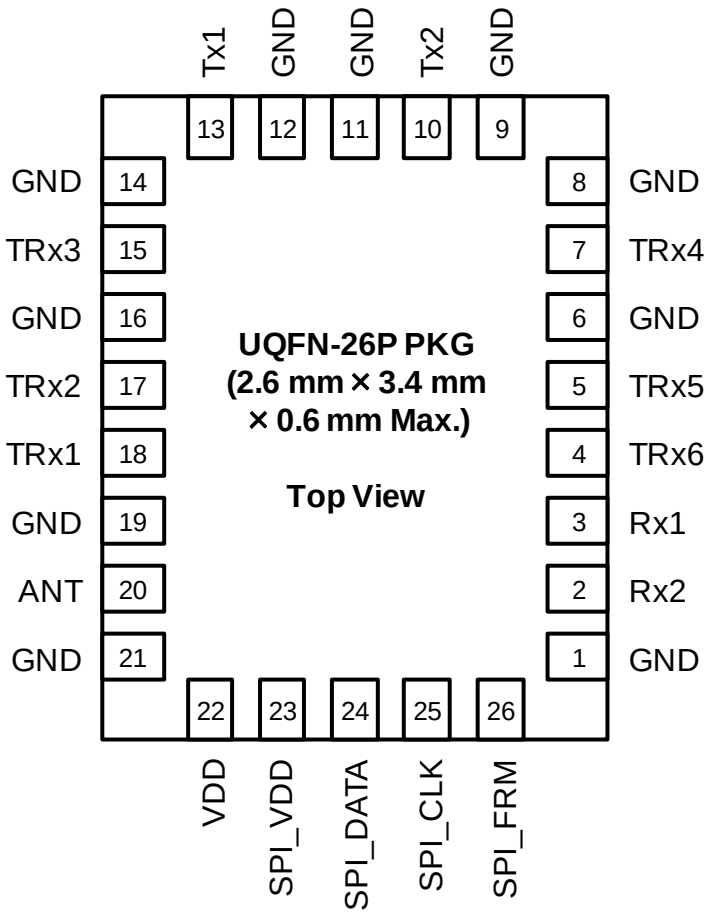
Truth Table

State	Active Path	SPI_Bit				SW State(*1)																			
		D14	D13	D12	D11	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	F19	F20
1	Tx1	0	0	1	0	H	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H
2	Tx2	0	0	0	1	L	H	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H
3	TRx1	0	1	0	0	L	L	H	L	L	L	L	L	L	L	H	H	L	H	H	H	H	H	H	H
4	TRx2	0	1	0	1	L	L	L	H	L	L	L	L	L	L	H	H	H	L	H	H	H	H	H	H
5	TRx3	0	1	1	0	L	L	L	L	H	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H
6	TRx4	1	0	0	0	L	L	L	L	L	H	L	L	L	L	H	H	H	H	H	L	H	H	H	H
7	TRx5	1	0	0	1	L	L	L	L	L	L	H	L	L	L	H	H	H	H	H	H	L	H	H	H
8	TRx6	1	0	1	0	L	L	L	L	L	L	L	H	L	L	H	H	H	H	H	H	H	L	H	H
9	Rx1	1	1	0	0	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	L	H
10	Rx2	1	1	0	1	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L
11	Idle(*2)	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
12	Isolation	1	1	1	1	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H

(*1) State ”L” means a switch “OFF”, State ”H” means a switch “ON”

(*2) State “Idle” means that the DC/DC Converter is “OFF”, and the switch paths are in an undefined state.

Pin Configuration



DC Bias Conditions

Ta = 25 °C

Item	Min.	Typ.	Max.	Unit
Vdd	2.5	2.9	3.3	V
SPI_Vdd	1.35	1.8	1.98	V
SPI_Vctl (H)	SPI_Vdd × 0.7	—	SPI_Vdd + 0.3	V
SPI_Vctl (L)	-0.3	—	SPI_Vdd × 0.3	V

Electrical Characteristics

Vdd=2.5V , Ta=25 ℃

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL	Ant - TRx1	*1, *2, *3	-	0.47	0.57	dB
			*4	-	0.70	0.85	
			*5	-	0.80	0.95	
			*6	-	0.90	1.10	
			*7	-	1.20	1.40	
		Ant - TRx2	*1, *2, *3	-	0.47	0.57	
			*4	-	0.65	0.80	
			*5	-	0.70	0.85	
			*6	-	0.80	1.00	
			*7	-	1.00	1.20	
		Ant - TRx3	*1, *2, *3	-	0.47	0.57	
			*4	-	0.60	0.75	
			*5	-	0.65	0.80	
			*6	-	0.75	0.95	
			*7	-	1.00	1.20	
		Ant - TRx4	*1, *2, *3	-	0.45	0.55	
			*4	-	0.55	0.70	
			*5	-	0.60	0.75	
			*6	-	0.70	0.90	
			*7	-	0.95	1.15	
		Ant - TRx5	*1, *2, *3	-	0.47	0.57	
			*4	-	0.70	0.85	
			*5	-	0.75	0.90	
			*6	-	0.80	1.00	
			*7	-	1.00	1.20	
		Ant - TRx6	*1, *2, *3	-	0.47	0.57	
			*4	-	0.65	0.80	
			*5	-	0.70	0.85	
			*6	-	0.80	1.00	
			*7	-	1.05	1.25	
		Ant - Tx1	*8	-	1.15	1.30	
		Ant - Tx2	*9	-	1.15	1.35	
		Ant - Rx1	*10	-	0.75	0.85	
			*11	-	0.90	1.05	
		Ant - Rx2	*10	-	0.75	0.85	
			*11	-	0.90	1.05	

Vdd=2.5 V , Ta=25 ℃

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Isolation	ISO	Tx1 - TRx1, 2, 3, 4, 5, 6, Rx1, 2 (Tx1 Active)	*8	35	-	-	dB
		Tx2 - TRx1, 2, 3, 4, 5, 6, Rx1, 2 (Tx2 Active)	*9	32	-	-	
		TRx1, 2, 3 - TRx4, 5, 6 (The port of the input is Active.)	600 to 2170 MHz	35	-	-	
		TRx1 - TRx2 (TRx1 or TRx2 Active)	600 to 2170 MHz	20	-	-	
		TRx1 - TRx3 (TRx1 or TRx3 Active)	600 to 2170 MHz	30	-	-	
		TRx2 - TRx3 (TRx2 or TRx3 Active)	600 to 2170 MHz	25	-	-	
		TRx4 - TRx5 (TRx4 or TRx5 Active)	600 to 2170 MHz	25	-	-	
		TRx4 - TRx6 (TRx4 or TRx6 Active)	600 to 2170 MHz	30	-	-	
		TRx5 - TRx6 (TRx5 or TRx6 Active)	600 to 2170 MHz	20	-	-	
VSWR	VSWR	All Ports in Active Paths	600 to 2170 MHz	-	-	1.50	-
Harmonics	2fo	Ant - TRx1, 2, 3, 4, 5, 6	*3, *4	-	-	-39	dBm
	3fo			-	-	-39	
	2fo	Ant - Tx1	*8	-	-	-36	
	3fo			-	-	-35	
	2fo	Ant - Tx2	*9	-	-	-33	
	3fo			-	-	-33	
Attenuation	ATT	Tx1 - Ant	1648 to 1805 MHz	25	-	-	dB
			1805 to 1830 MHz	30	-	-	
			2472 to 2745 MHz	25	-	-	
			2745 to 4575 MHz	20	-	-	
			4575 to 6405 MHz	15	-	-	
			6405 to 12750 MHz	20	-	-	
		Tx2 - Ant	3420 to 3820 MHz	25	-	-	
			5130 to 5730 MHz	25	-	-	
			5730 to 12750 MHz	20	-	-	
Inter Modulation Product Power in Rx Band	IMD2	Ant - TRx1, 2, 3, 4, 5, 6	*12, 13, 14, 17, 18, 21, 22	-	-	-107	dBm
	IMD3		*12, 15, 16, 19, 20, 23, 24	-	-	-107	
Input IP3	IIP3	Ant - TRx1, 2, 3, 4, 5, 6	*12, 25, 26	65	68	-	dBm
Switching Time	Ts	Active Mode	50 % Ctl to 90 % RF	-	3	5	µs
Wake Up Time	Tw		Wake Up Time from Idle Mode to Active Mode	-	30	50	µs
Supply Current	Idd	Active Mode	Vdd=2.5 V	-	-	0.40	mA
		Idle Mode	Vdd=2.5 V	-	-	20	µA

Electrical Characteristics are measured with all RF ports terminated in 50 Ω.

Corresponding Band of TRx(UMTS/CDMA)

*1 Pin = 26 dBm, 452 to 468 MHz (Band Class 5)

*2 Pin = 25 dBm, 704 to 787 MHz (Band 13, Band 17)

*3 Pin = 26 dBm, 824 to 960 MHz (Band 5, Band 8)

*4 Pin = 26 dBm, 1710 to 1990 MHz (Band 1 Tx, Band 2 Tx, Band 3 Tx, Band4 Tx)

*5 Pin = 10 dBm, 2110 to 2170 MHz (Band 1 Rx, Band 4 Rx)

*6 Pin = 26 dBm, 2300 to 2400 MHz (Band 40)

*7 Pin = 26 dBm, 2500 to 2690 MHz (Band 7)

*8 Pin = 35 dBm, 824 to 915 MHz (GSM850/900 Tx)

*9 Pin = 32 dBm, 1710 to 1910 MHz (GSM1800/1900 Tx)

*10 Pin = 10 dBm, 869 to 960 MHz (GSM850/900 Rx)

*11 Pin = 10 dBm, 1805 to 1990 MHz (GSM1800/1900 Rx)

*12 Measured with the recommended circuit

IMD Condition

Band	fRx on TRx	fTx +20 dBm on TRx	fBlocker -15 dBm on Ant		IMD Condition
Band I	2140 MHz	1950 MHz	IMD2(fRx - fTx)	190 MHz	*13
			IMD2(fRx + fTx)	4090 MHz	*14
			IMD3(2fTx - fRx)	1760 MHz	*15
			IMD3(2fTx + fRx)	6040 MHz	*16
Band II	1960 MHz	1880 MHz	IMD2(fRx - fTx)	80 MHz	*17
			IMD2(fRx + fTx)	3840 MHz	*18
			IMD3(2fTx - fRx)	1800 MHz	*19
			IMD3(2fTx + fRx)	5720 MHz	*20
Band V	880 MHz	835 MHz	IMD2(fRx - fTx)	45 MHz	*21
			IMD2(fRx + fTx)	1715 MHz	*22
			IMD3(2fTx - fRx)	790 MHz	*23
			IMD3(2fTx + fRx)	2550 MHz	*24

IIP3 Condition

Band	f1 +27 dBm on TRx	f2 +27 dBm on TRx	IIP3 Condition IIP3=(3*Pout-IM3)/2
Band I	1950 MHz	1951 MHz	*25
Band V	835 MHz	836 MHz	*26

Triple Beat Ratio

Vdd=2.5 V , Ta=25 ℃

Item	Symbol	Path	Condition				Min.	Typ.	Max.	Unit
			Tx1 at TRx* 21.5dBm	Tx2 at TRx* 21.5dBm	Jammer at Ant -30dBm	Triple Beat Product at TRx*				
Triple Beat Ratio	TBR	Ant - TRx1, 2, 3, 4, 5, 6	835.5 MHz	836.5 MHz	881.5 MHz	881.5±1 MHz	81	-	-	dBc
			1880 MHz	1881 MHz	1960 MHz	1960±1 MHz	81	-	-	

Electrical Characteristics are measured with all RF ports terminated in 50 Ω.

Measured with the recommended circuit

Input IP2

Vdd=2.5 V , Ta=25 ℃

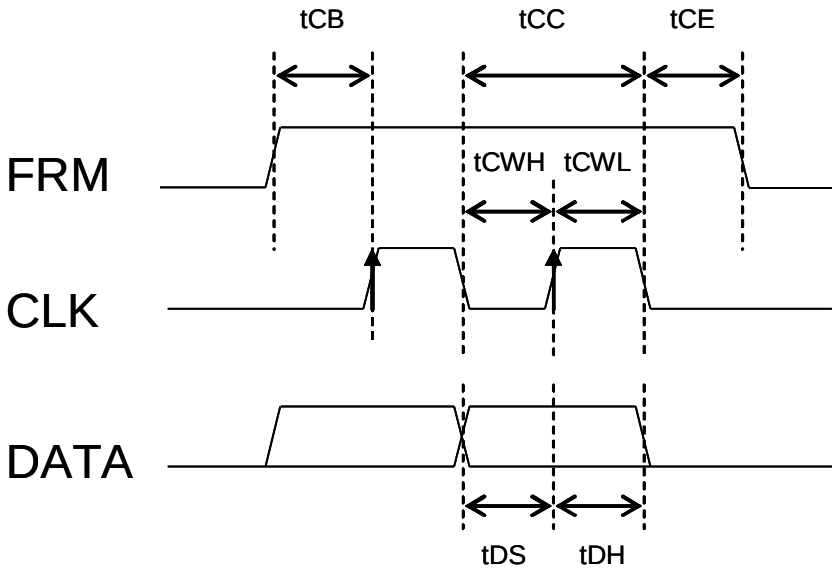
Item	Symbol	Path	Condition			Min.	Typ.	Max.	Unit
			Tx at TRx* 24dBm	Jammer at Ant -20dBm	IM2 Product at TRx*				
Input IP2	IIP2	Ant - TRx1, 2, 3, 4, 5, 6	836.61	1718.61	881.61	113.5	-	-	dBm
			836.61	45	881.61	95.5	-	-	
			1885	3850	1965	95.5	-	-	
			1885	80	1965	95.5	-	-	
			1732.5	3865	2132.5	95.5	-	-	
			1732.5	400	2132.5	95.5	-	-	

Electrical Characteristics are measured with all RF ports terminated in 50 Ω.

Measured with the recommended circuit

SPI Timing Characteristic

Item	Unit	Condition	SPEC			Unit
			Min.	Typ.	Max.	
SPI Bias Current	SPI_Idd	SPI_Vdd=1.8 V	-	200	400	µA
SPI Ctrl Current	SPI_Ictl	SPI_Vdd=1.8 V	-	-	10	µA
SPI_Enable	SPI_EN	SPI_Vdd↑(90 %) to SPI_FRM↑	10	-	-	µs
Clock Freaquency	CLK_Freq	SPI_Vdd Enable	-	-	26	MHz
Clock Cycle	tCC	CLK_Freq=26 MHz	34	38.4	42	ns
Clock Begin Time	tCB		tCC/2	-	-	ns
Clock End Time	tCE		tCC/2	-	-	ns
Clock Width H	tCWH		tCCx0.4	-	-	ns
Clock Width L	tCWL		tCCx0.4	-	-	ns
Data Setup Time	tDS		5	-	-	ns
Data Hold Time	tDH		5	-	-	ns
SPI_Vdd rise time	T_{SPI_Vdd} Rise	10 % to 90 % SPI_Vdd	2.2	-	-	µs



SPI Control Specification

Parameter	Specification
Address bits	14 bits
Data bits	16 bits
Total bits	30 bits total
Clock Edge(data sampling)	Rising Edge

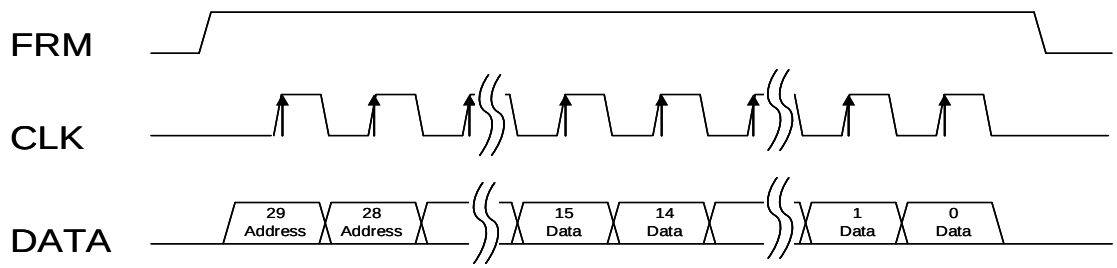
Address		Control Data	
29	16	15	0
MSB			LSB

Port Symbol	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	R/W	Device address								Register address				
Idle	0	0	0	0	1	0	0	0	1	0	0	0	0	0
Tx1	0	0	0	0	1	0	0	0	1	0	0	0	0	0
Tx2	0	0	0	0	1	0	0	0	1	0	0	0	0	0
TRx1	0	0	0	0	1	0	0	0	1	0	0	0	0	0
TRx2	0	0	0	0	1	0	0	0	1	0	0	0	0	0
TRx3	0	0	0	0	1	0	0	0	1	0	0	0	0	0
TRx4	0	0	0	0	1	0	0	0	1	0	0	0	0	0
TRx5	0	0	0	0	1	0	0	0	1	0	0	0	0	0
TRx6	0	0	0	0	1	0	0	0	1	0	0	0	0	0
Rx1	0	0	0	0	1	0	0	0	1	0	0	0	0	0
Rx2	0	0	0	0	1	0	0	0	1	0	0	0	0	0
Isolation	0	0	0	0	1	0	0	0	1	0	0	0	0	0
Idle	0	1	1	1	1	1	1	1	1	1	1	1	1	1

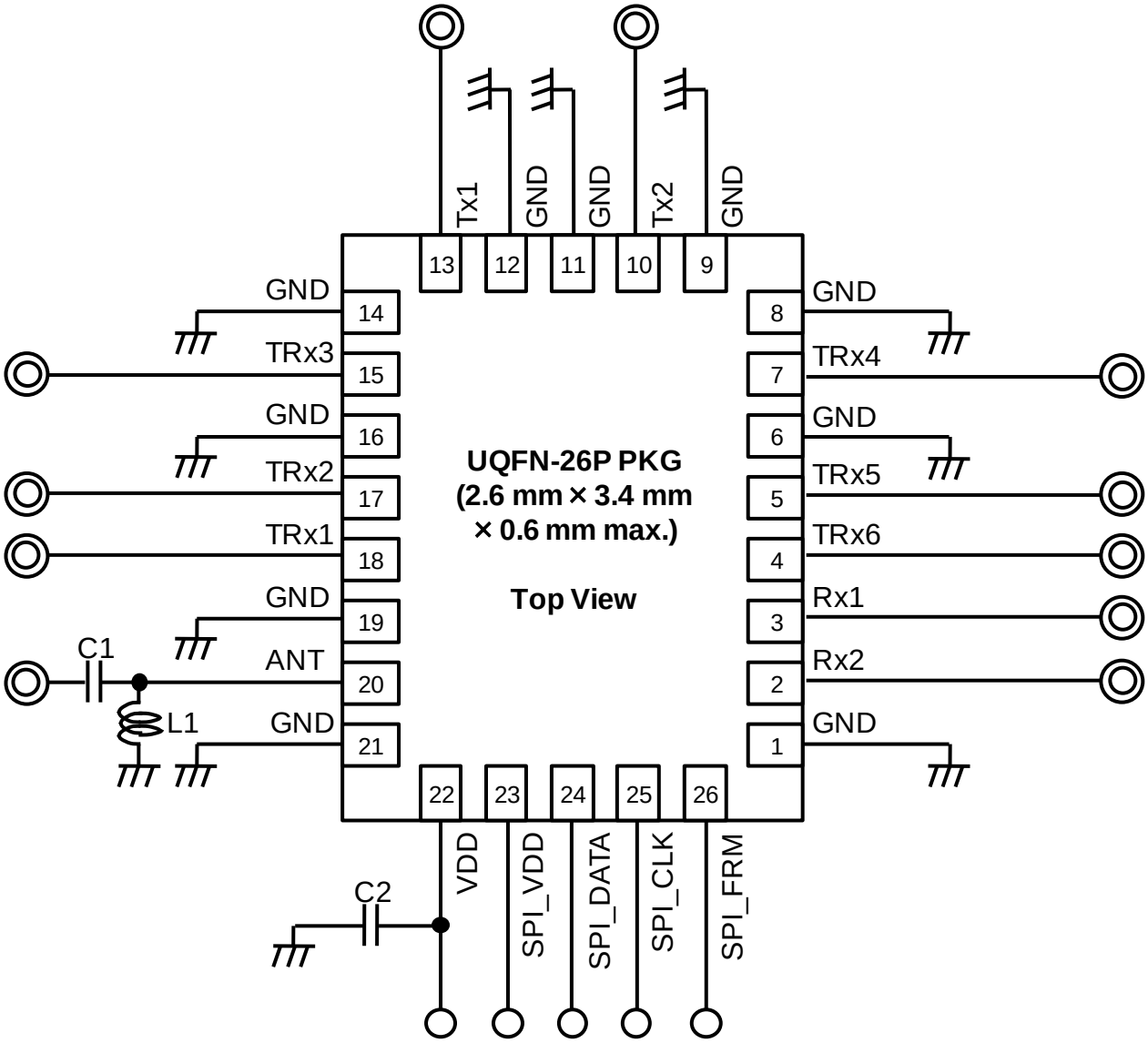
Port Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data															
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Idle	x	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x
Tx1	x	0	0	1	0	x	x	x	x	x	x	x	x	x	x	x
Tx2	x	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x
TRx1	x	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x
TRx2	x	0	1	0	1	x	x	x	x	x	x	x	x	x	x	x
TRx3	x	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x
TRx4	x	1	0	0	0	x	x	x	x	x	x	x	x	x	x	x
TRx5	x	1	0	0	1	x	x	x	x	x	x	x	x	x	x	x
TRx6	x	1	0	1	0	x	x	x	x	x	x	x	x	x	x	x
Rx1	x	1	1	0	0	x	x	x	x	x	x	x	x	x	x	x
Rx2	x	1	1	0	1	x	x	x	x	x	x	x	x	x	x	x
Isolation	x	1	1	1	1	x	x	x	x	x	x	x	x	x	x	x
Idle	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

*Either idle state D11-D14 is 0000, or XXXX

Clock Block Diagram



Recommended Circuit



*1: No DC blocking capacitors are required on all RF ports. (Except sourcing DC bias)

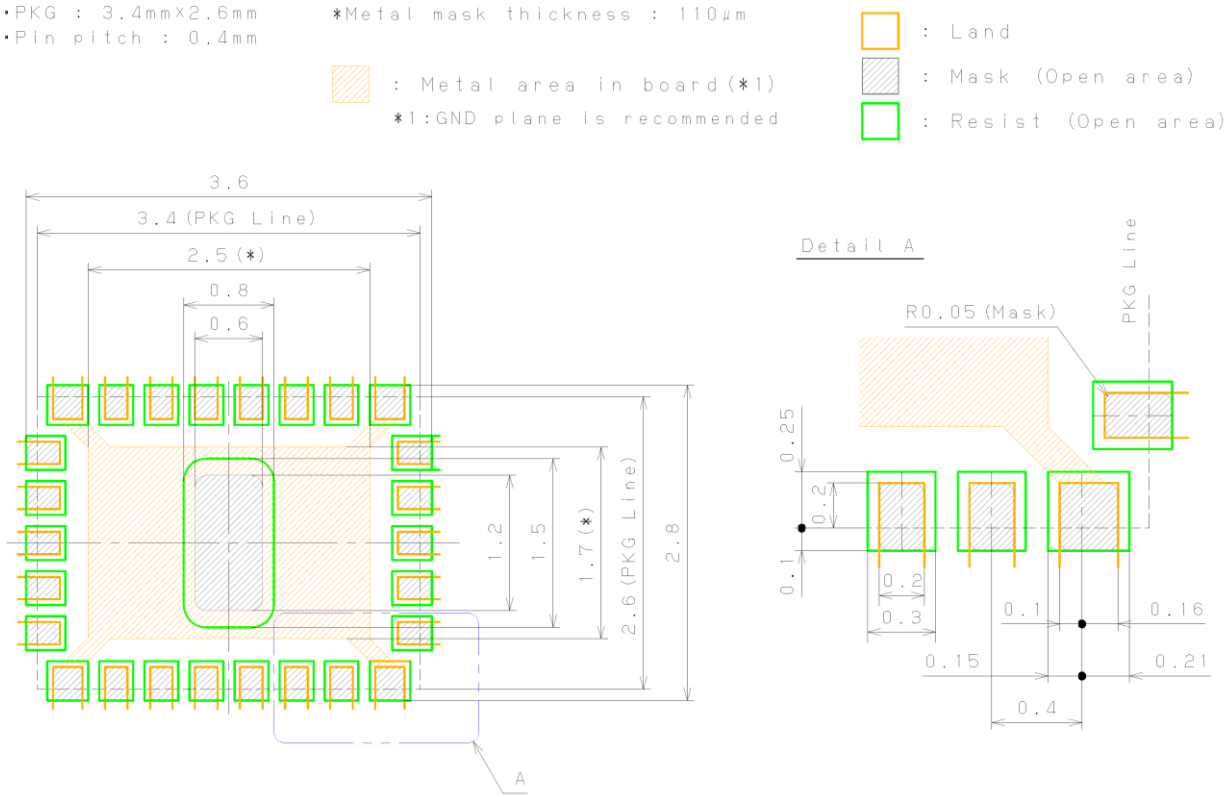
*2: DC levels of all RF ports are GND.

*3: L1(22 nH) and C1(22 pF) are recommended on Ant port for ESD protection.

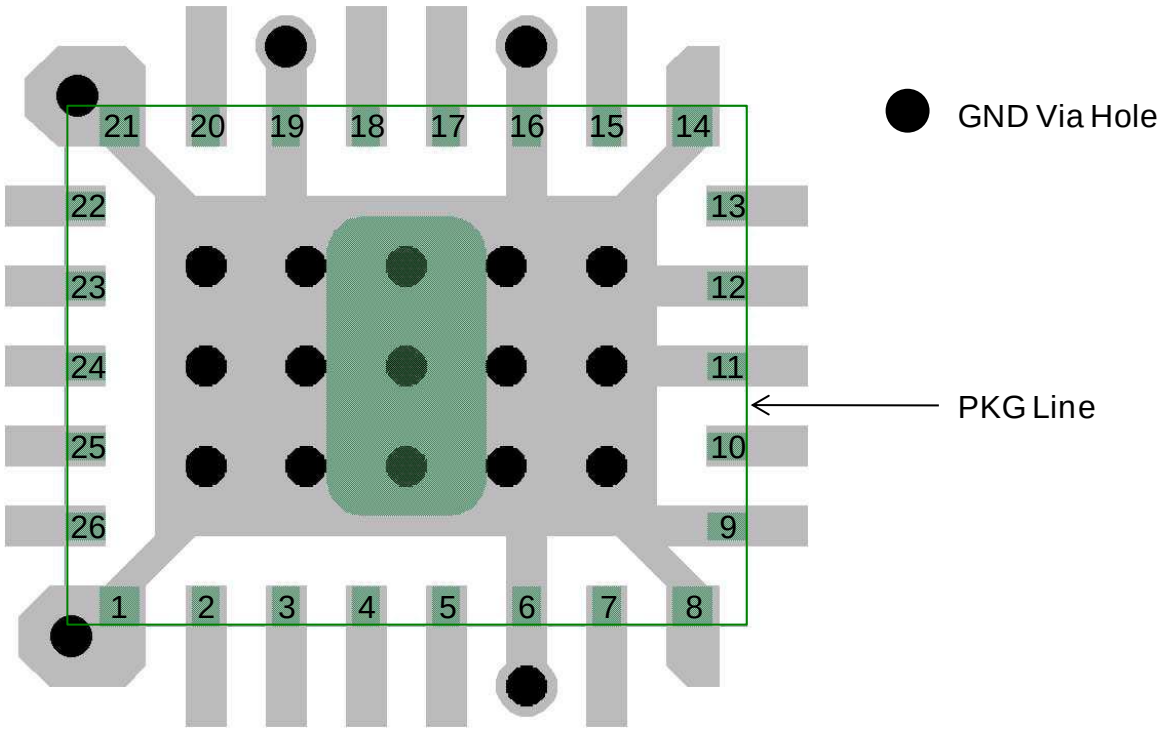
*4: C2(100 pF) is recommended.

PCB Layout

Foot Pattern



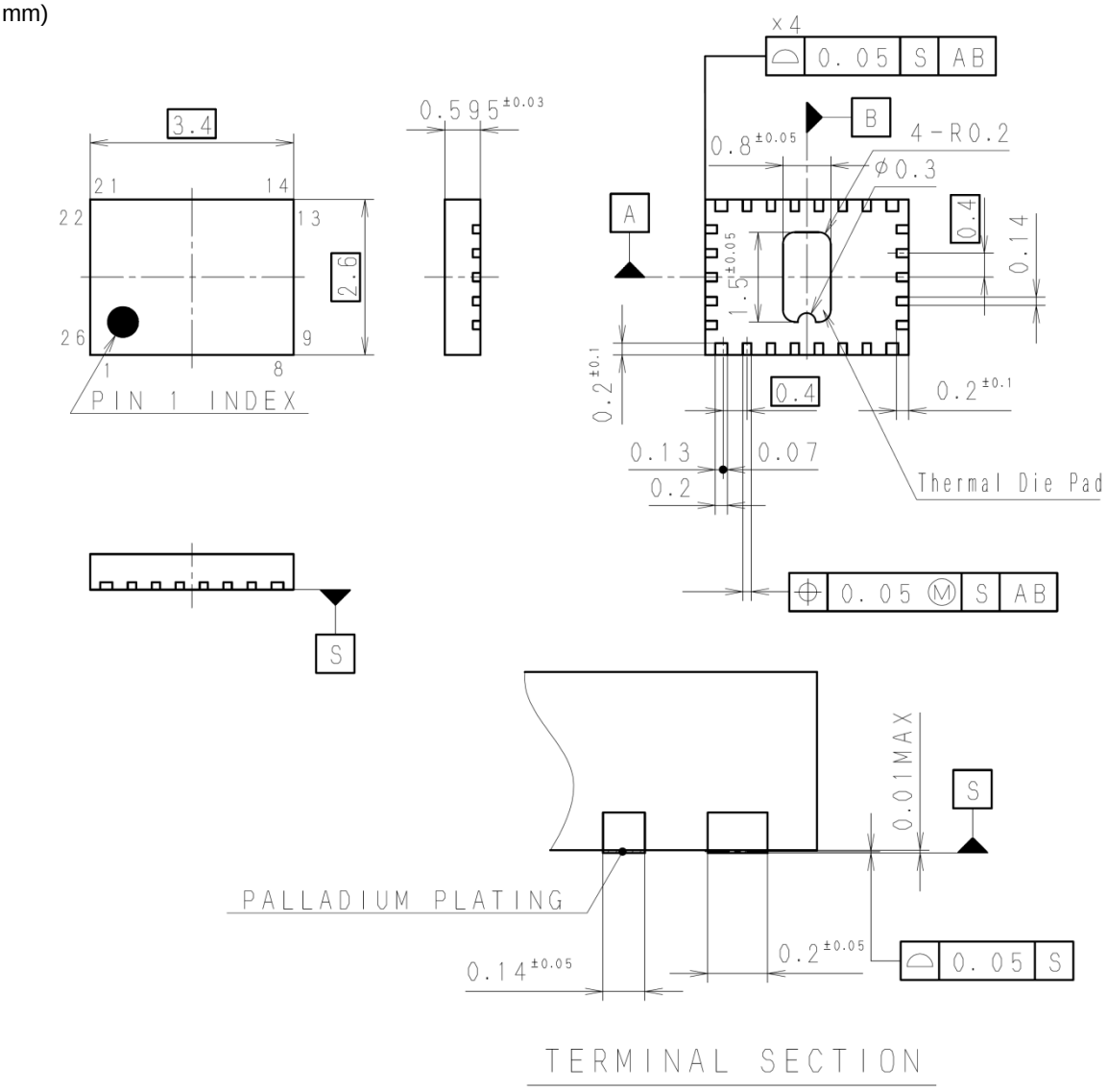
Recommended PCB Design



Package Outline

Product Code: 875341595, 875341837(Katoh)

(Unit: mm)



Note:Terminal burr height 0.05mm MAX.

SONY CODE	UQFN-26P-541
JEITA CODE	————
JEDEC CODE	————

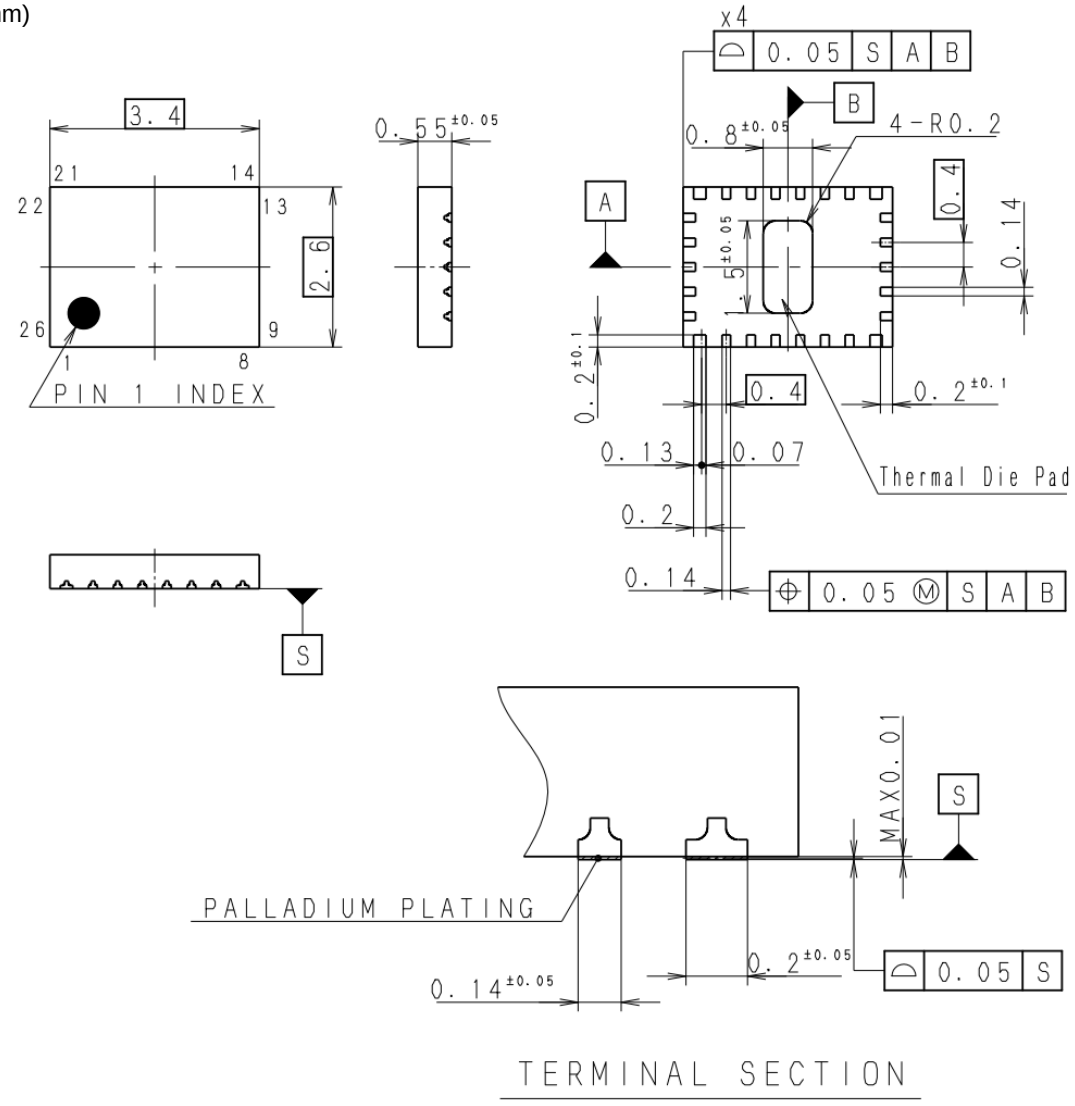
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.013g

Package Outline

Product Code: 875342248, 875342253(SDT-Bangna)

(Unit: mm)



TERMINAL SECTION

Note:Terminal burr height 0.05mm MAX.

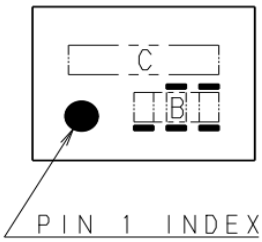
SONY CODE	UQFN-26P-01
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.013g

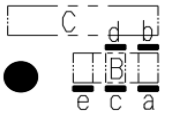
Marking

Product Code: 875341595, 875341837(Katoh)



MARKING C: M3588

注1） B部はロット番号（Ｍａｘ３文字で通し記号）を配置する。
（規定文字数未満につき省略は省略規定に従う。
製造年は下記２進法ビット方式により表示する。）
ａ部年コード（２進法ビット方式の１ビット目を表示）を配置する。
ｂ部年コード（２進法ビット方式の２ビット目を表示）を配置する。
ｃ部年コード（２進法ビット方式の３ビット目を表示）を配置する。
ｄ部年コード（２進法ビット方式の４ビット目を表示）を配置する。
注2） C部は製品名（Ｍａｘ５文字）を配置する。
（５文字を超える場合は製品名省略標示規定に従う。）
注3） ｅ部は組立場所表記を配置する。

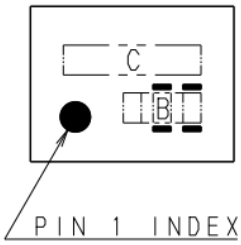


DETAIL B

< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
(FOLLOW RULES FOR ABBREVIATIONS.
MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)
A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION a.
A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION b.
A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION c.
A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION d.
2) TYPE NO. (MAX 5 CHARACTERS) IN SECTION C.
(FOR MORE THAN 5 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) ASSEMBLY PLACE IN SECTION e.

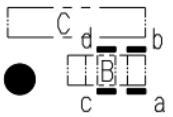
Marking

Product Code: 875342248, 875342253(SDT-Bangna)



MARKING C: M3588

注1） B部はロット番号（Ｍａｘ３文字で通し記号）を配置する。
（規定文字数未満につき省略は省略規定に従う。
製造年は下記２進法ビット方式により表示する。）
ａ部年コード（２進法ビット方式の１ビット目を表示）を配置する。
ｂ部年コード（２進法ビット方式の２ビット目を表示）を配置する。
ｃ部年コード（２進法ビット方式の３ビット目を表示）を配置する。
ｄ部年コード（２進法ビット方式の４ビット目を表示）を配置する。
注2） C部は製品名（Ｍａｘ５文字）を配置する。
（５文字を超える場合は製品名省略標示規定に従う。）
注3） マーク深さは、ＭＡＸ０．０５ｍｍの事.



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2) TYPE NO. (MAX 5 CHARACTERS) IN SECTION C.
(FOR MORE THAN 5 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) MARK DEPTH MAX 0.05 mm

Note

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Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits