DATA SHEET

PCA9557

8-bit I^2C and SMBus I/0 port with reset

Product data

2001 Dec 12

File under Integrated Circuits — ICL03

Philips
Semiconductors

PHILIPS

8-bit I²C and SMBus I/0 port with reset PCA9557

FEATURES

- Lower voltage, higher performance migration path for the PCA9556
- 8 general purpose input/output expander/collector
- Input/output configuration register
- Active HIGH polarity inversion register
- I²C and SMBus interface logic
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- Active LOW reset input
- 3 address pins allowing up to 8 devices on the I²C/SMBus
- High impedance open drain on I/O0
- No glitch on power-up
- Power-up with all channels configured as inputs
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant inputs/outputs
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Package offer: SO 16, TSSOP 16

DESCRIPTION

The PCA9557 is a silicon CMOS circuit which provides parallel input/output expansion for SMBus and I²C applications. The PCA9557 consists of an 8-bit input port register, 8-bit output port register, and an I²C/SMBus interface. It has low current consumption and a high impedance open drain output pin, I/O0.

The system master can enable the PCA9557's I/O as either input or output by writing to the configuration register.

The system master can also invert the PCA9557 inputs by writing to the active HIGH polarity inversion register.

Finally, the system master can reset the PCA9557 in the event of a timeout by asserting a LOW in the reset input.

The power-on reset puts the registers in their default state and initializes the I²C/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without depowering the part.

PIN CONFIGURATION

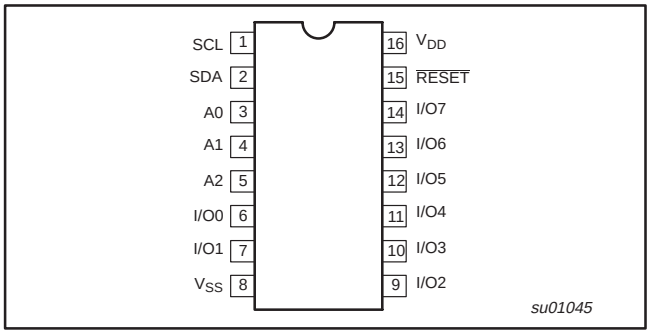


Figure 1. Pin configuration

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	SCL	Serial clock line
2	SDA	Serial data line
3	A0	Address input 0
4	A1	Address input 1
5	A2	Address input 2
6	I/O0	I/O0 (open drain)
7	I/O1	I/O1
8	V_{SS}	Supply ground
9	I/O2	I/O2
10	I/O3	I/O3
11	I/O4	I/O4
12	I/O5	I/O5
13	I/O6	I/O6
14	I/O7	I/O7
15	$\overline{\text{RESET}}$	Active low reset input
16	V_{DD}	Supply voltage

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
16-Pin Plastic SO (narrow)	–40 to +85 °C	PCA9557D	SOT109-1
16-Pin Plastic TSSOP	–40 to +85 °C	PCA9557PW	SOT403-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.
SMBus as specified by the Smart Battery System Implementers Forum is a derivative of the Philips I²C patent.
I²C is a trademark of Philips Semiconductors Corporation.

BLOCK DIAGRAM

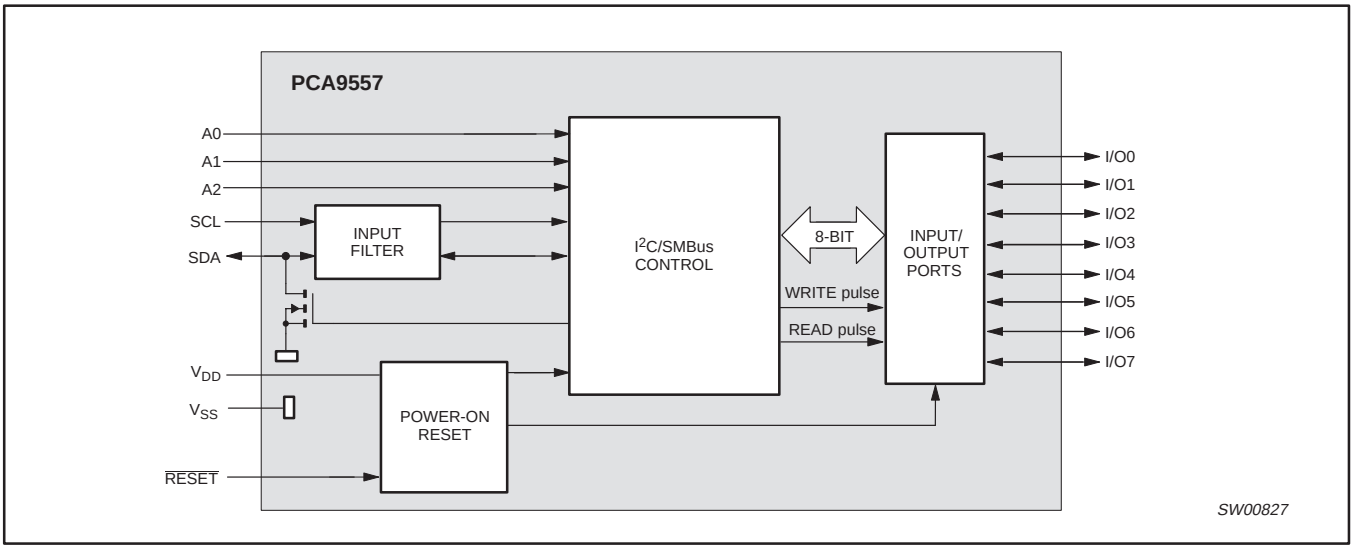


Figure 2. Block diagram

SYSTEM DIAGRAM

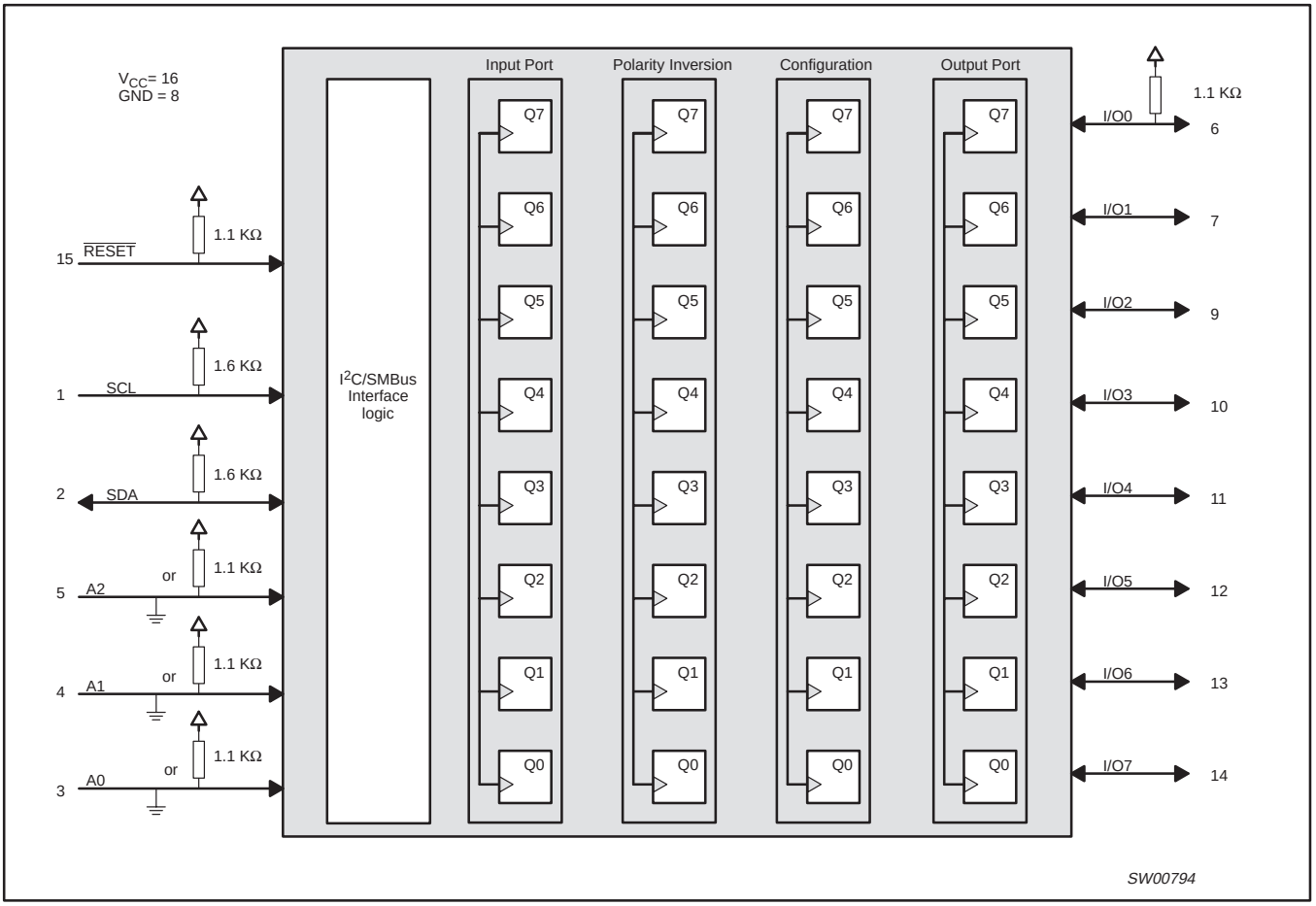
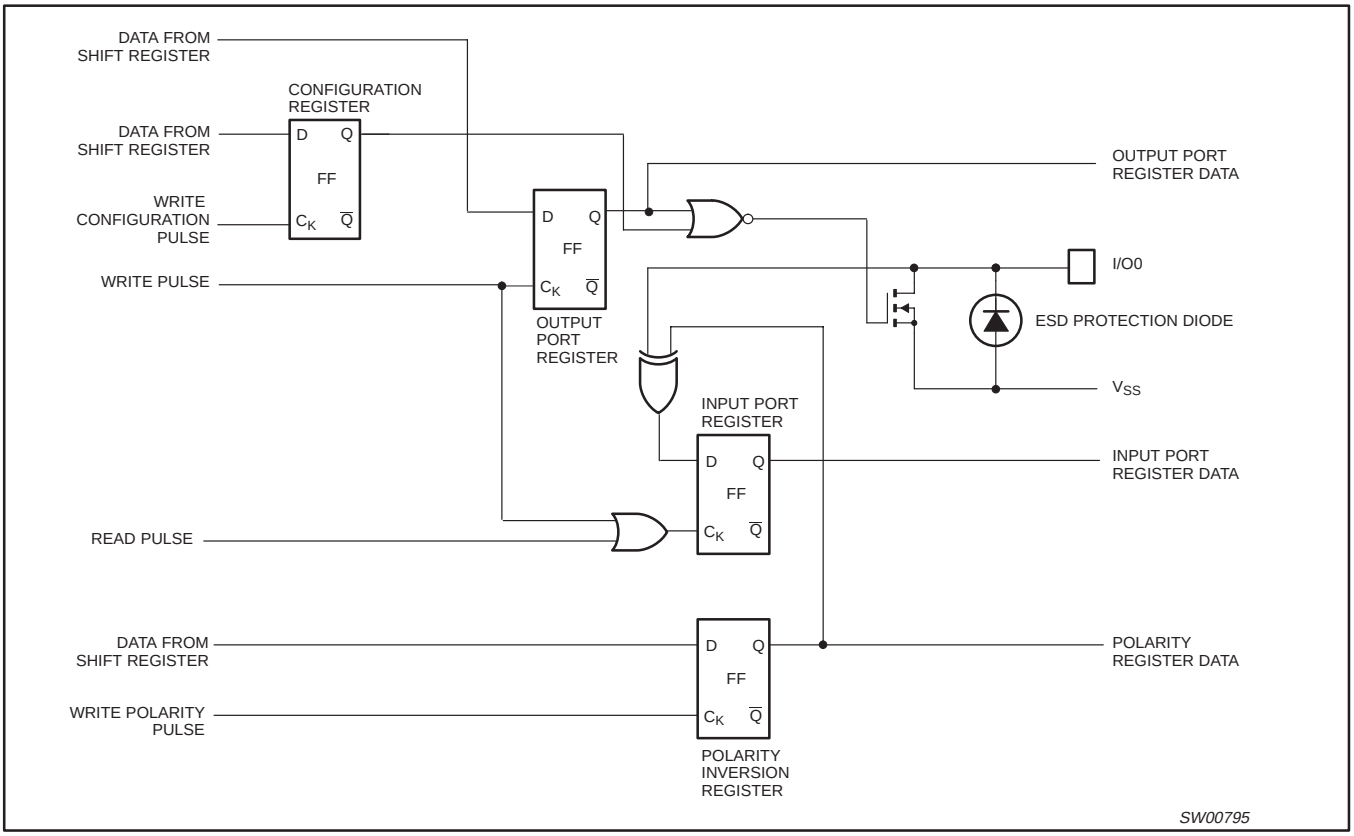


Figure 3. System diagram

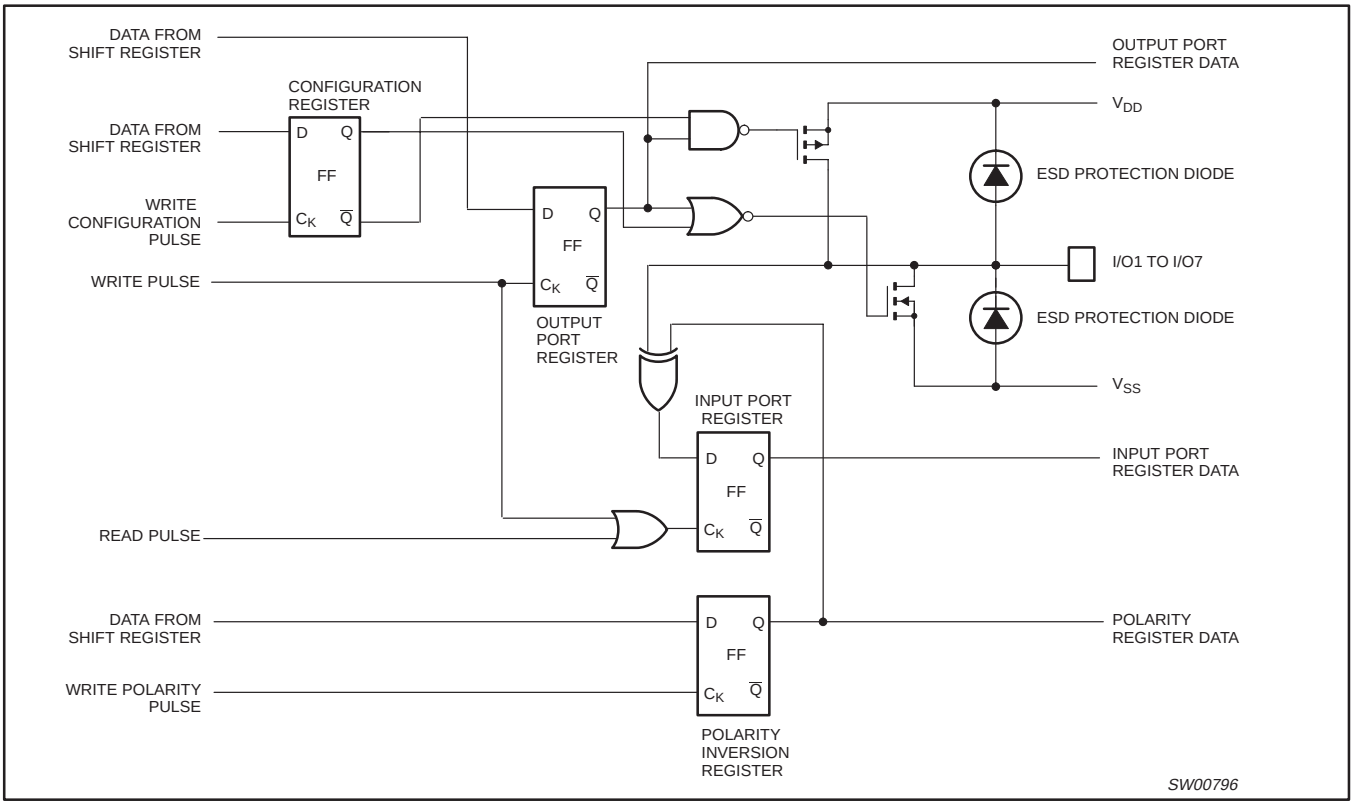
SIMPLIFIED SCHEMATIC OF I/O0



NOTE: On power–up or reset, all registers return to default values.

Figure 4. Simplified schematic of I/O0

SIMPLIFIED SCHEMATIC OF I/O1 TO I/O7



NOTE: On power–up or reset, all registers return to default values.

Figure 5. Simplified schematic of I/O1 to I/O7

DEVICE ADDRESS

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9557 is shown in Figure 6. To conserve power, no internal pullup resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

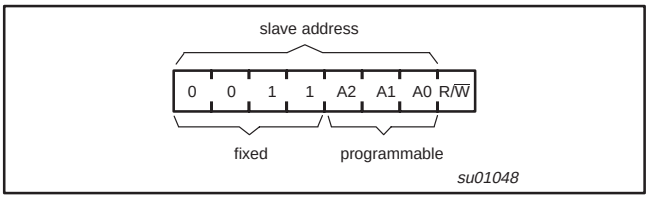


Figure 6. PCA9557 address

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read is selected while a logic 0 selects a write operation.

CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9557, which will be stored in the control register. This register can be written and read via the I²C bus.

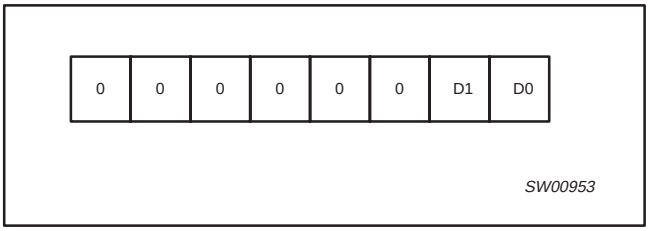


Figure 7. Control Register

REGISTER DEFINITION

D1	D0	NAME	TYPE	FUNCTION
0	0	Register 0	Read	Input port register
0	1	Register 1	Read/Write	Output port register
1	0	Register 2	Read/Write	Polarity inversion register
1	1	Register 3	Read/Write	Configuration register

REGISTER DESCRIPTION

Register 0 – Input Port Register

I7	I6	I5	I4	I3	I2	I1	I0

This register is an read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration Register. Writes to this register have no effect.

Register 1 – Output Port Register

bit	O7	O6	O5	O4	O3	O2	O1	O0
default	0	0	0	0	0	0	0	0

This register reflects the outgoing logic levels of the pins defined as outputs by the Configuration Register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

Register 2 – Polarity Inversion Register

bit	N7	N6	N5	N4	N3	N2	N1	N0
default	1	1	1	1	0	0	0	0

This register enables polarity inversion of pins defined as inputs by the Configuration Register. If a bit in this register is set (written with '1'), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a '0'), the corresponding port pin's original polarity is retained.

Register 3 – Configuration Register

bit	C7	C6	C5	C4	C3	C2	C1	C0
default	1	1	1	1	1	1	1	1

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output.

POWER-ON RESET

When power is applied to V_{DD}, an internal power-on reset holds the PCA9557 in a reset state until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9557 registers and I²C/SMBus state machine will initialize to their default states.

For a power reset cycle, V_{DD} must be set to 0 V, then ramped back to the operating voltage.

$\overline{\text{RESET}}$ INPUT

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of t_W. The PCA9557 registers and SMBus/I²C state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again HIGH. This input typically requires a pull-up to V_{CC}.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 8).

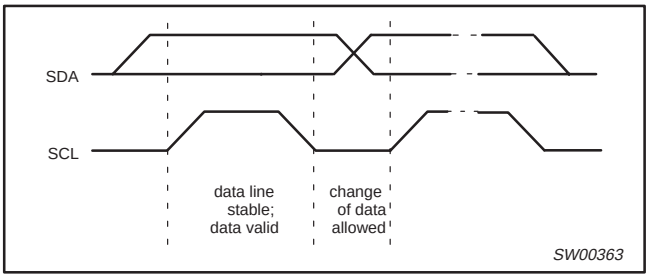


Figure 8. Bit transfer

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 9).

System configuration

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 10).

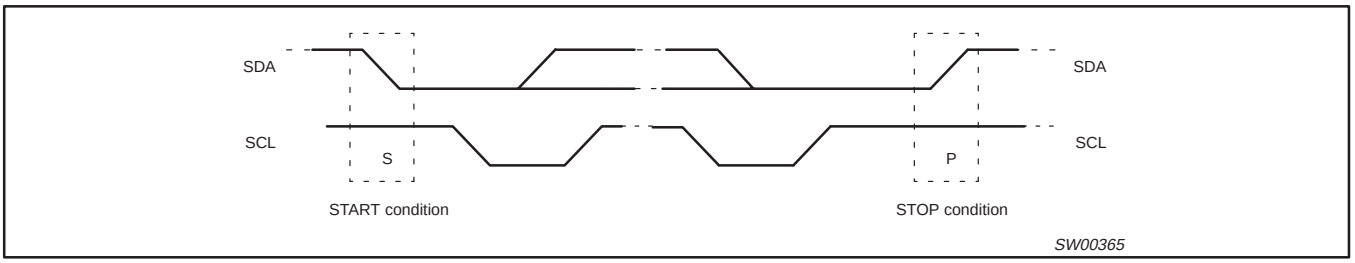


Figure 9. Definition of start and stop conditions

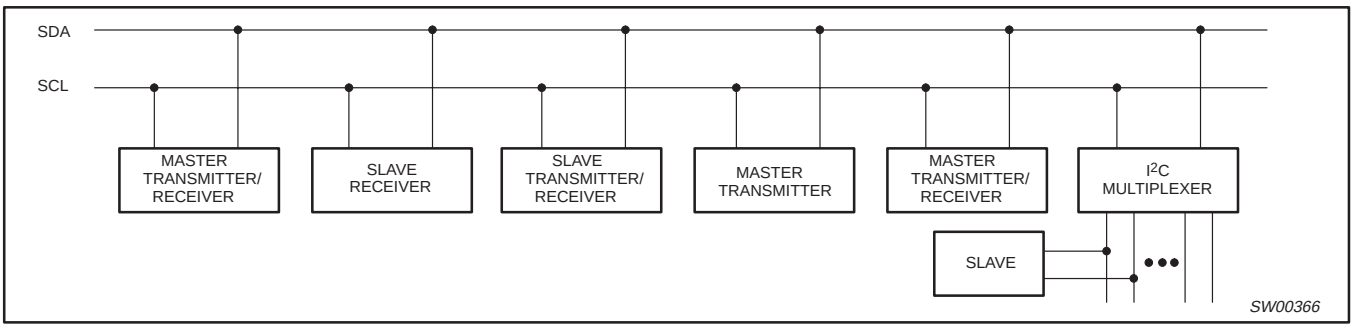


Figure 10. System configuration

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

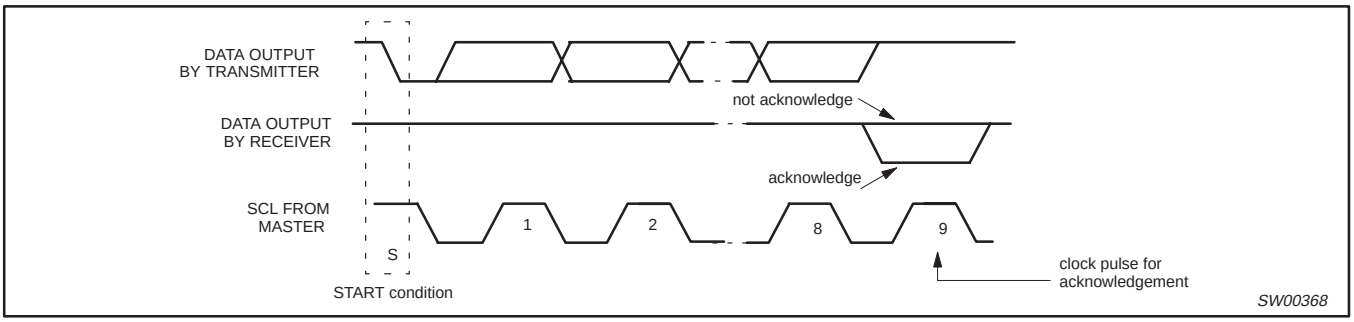


Figure 11. Acknowledgement on the I2C-bus

Bus Transactions

Data is transmitted to the PCA9557 registers using Write Byte transfers (see Figures 12 and 13). Data is read from the PCA9557 registers using Read and Receive Byte transfers (see Figures 14 and 15).

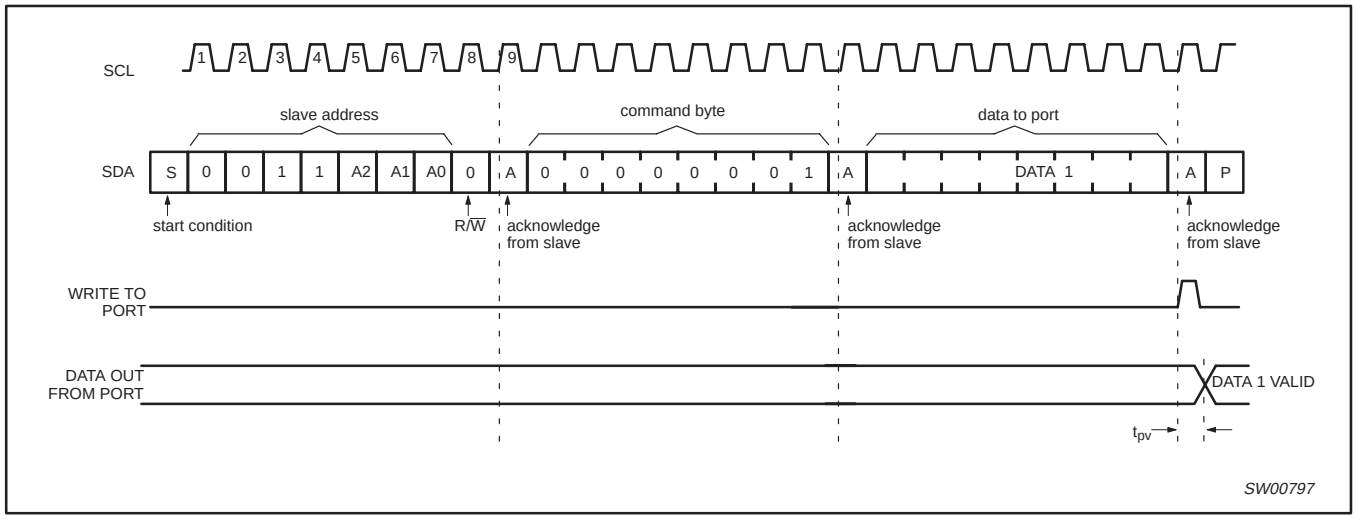


Figure 12. WRITE to output port register

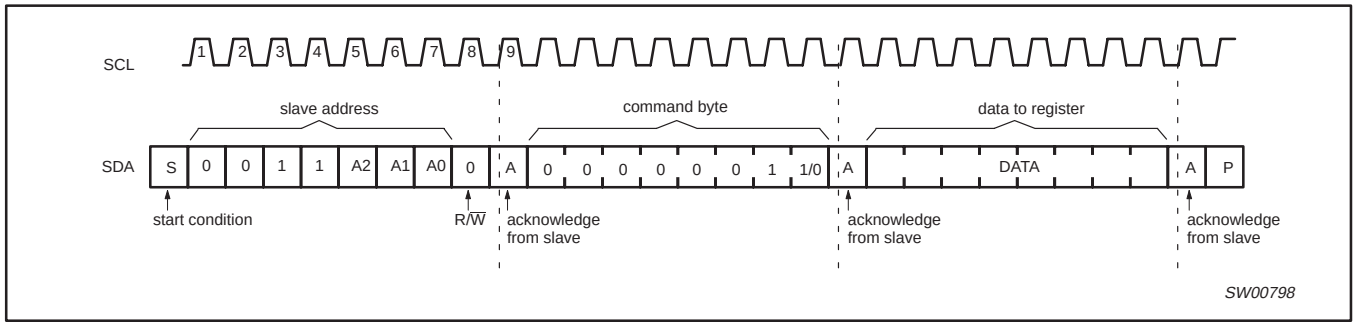


Figure 13. WRITE to I/O configuration or polarity inversion registers

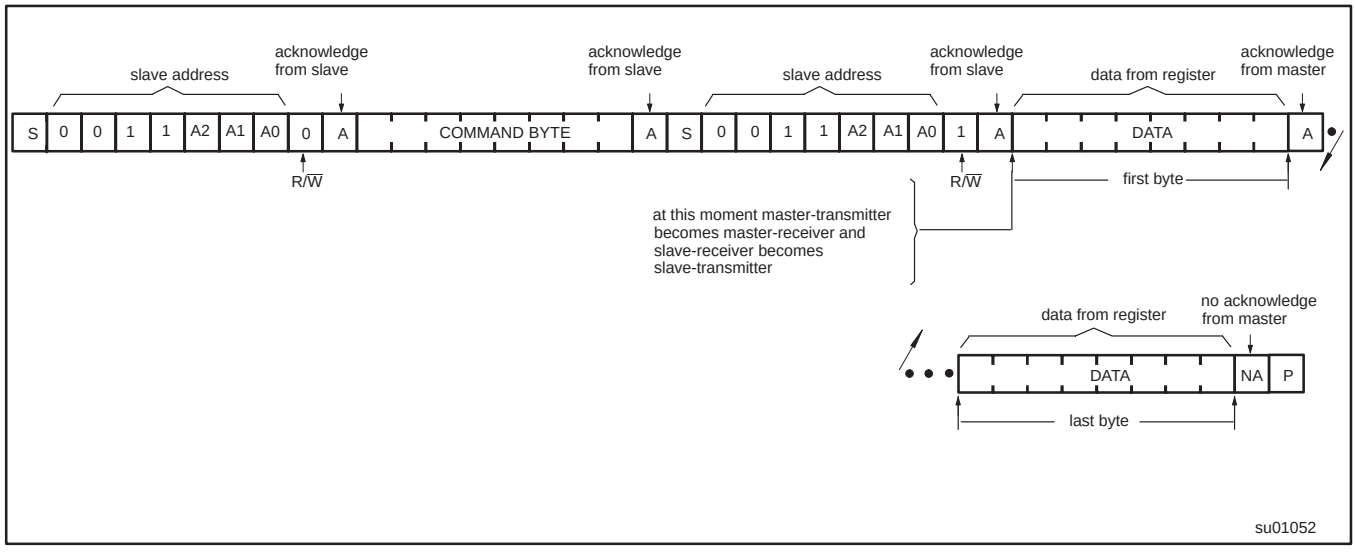
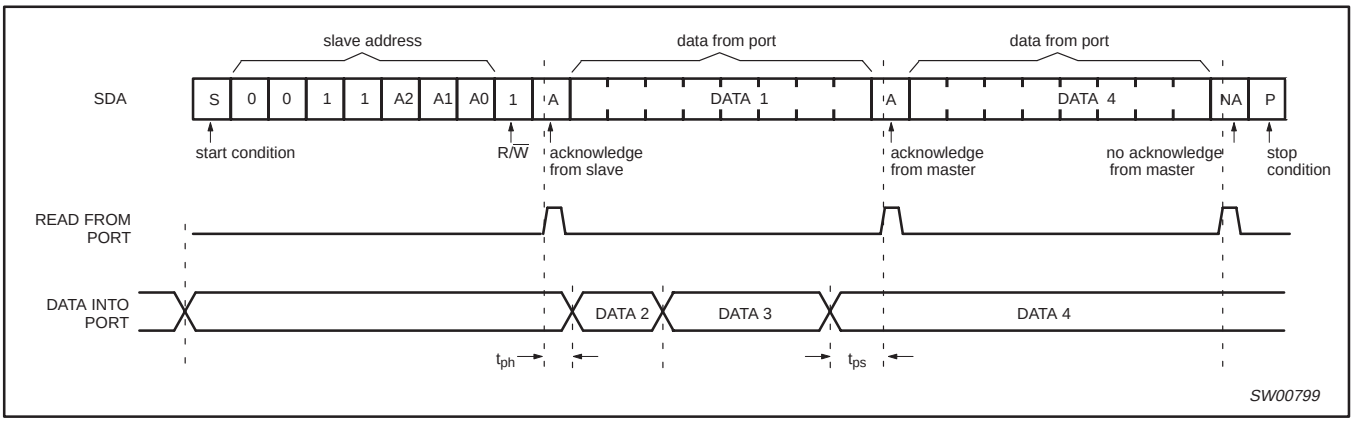


Figure 14. READ from register



NOTES:
1. This figure assumes the command byte has previously been programmed with 00h.
2. Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Figure 15. READ input port register

TYPICAL APPLICATION

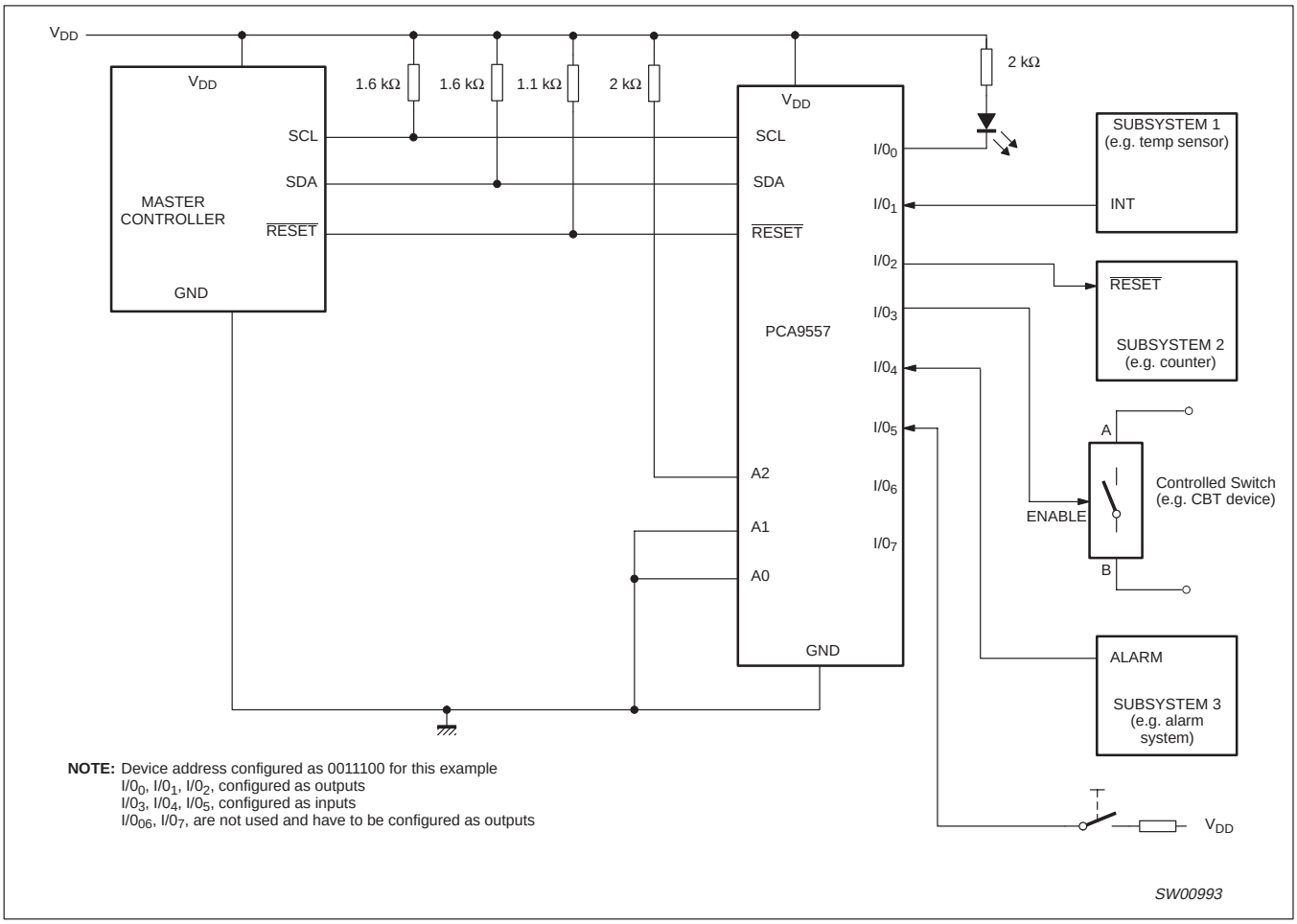


Figure 16. Typical application

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	DC supply voltage		–0.5	+6	V
V_I	DC input voltage		V_{SS} – 0.5	5.5	V
I_I	DC input current		—	± 20	mA
$I_{IHL(max)}$	Maximum allowed input current through protection diode (I/O1 – I/O7)	$V_I \geq V_{DD}$ or $V_I \leq V_{SS}$	—	±400	μA
$V_{I/O}$	DC voltage on an I/O as an input other than I/O0		V_{SS} – 0.5	5.5	V
$V_{I/O0}$	DC voltage on I/O0 as an input		V_{SS} – 0.5	5.5	V
$I_{I/O0}$	DC input current on I/O0		—	+400	μA
			—	–20	mA
$I_{I/O}$	DC output current on an I/O		—	± 50	mA
I_{DD}	DC supply current		—	85	mA
I_{SS}	DC supply current		—	100	mA
P_{tot}	Total power dissipation		—	200	mW
T_{stg}	Storage temperature range		–65	+150	°C
T_{amb}	Operating ambient temperature		–40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under ”*Handling MOS devices*”.

DC CHARACTERISTICS

V_{DD} = 2.3 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supplies						
V_{DD}	Supply voltage		2.3	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 3.6 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 kHz	—	—	1	µA
I_{stbl}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{SS}$; f_{SCL} = 0 kHz; I/O = inputs	—	—	1	µA
I_{stbh}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$; f_{SCL} = 0 kHz; I/O = inputs	—	—	1	µA
V_{POR}	Power-on reset voltage	No load; Temp = 25 °C $V_I = V_{DD}$ or V_{SS}	—	1.65	—	V
Input SCL; input/output SDA						
V_{IL}	LOW level input voltage		–0.5	—	0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	—	5.5	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	—	—	mA
I_L	Leakage current	$V_I = V_{DD}$ or V_{SS}	–1	—	+1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	6	10	pF
I/Os						
V_{IL}	LOW level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH level input voltage		2.0	—	5.5	V
I_{OL}	LOW level output current	V_{OL} = 0.55 V; note 1	8	10	—	mA
I_{OH}	HIGH level output current except I/O0	V_{OH} = 2.4 V; note 2	4	—	—	mA
	HIGH level output current on I/O0	V_{OH} = 4.6 V	—	—	1	µA
		V_{OH} = 3.3 V	—	—	1	
I_L	Input leakage current	V_{DD} = 5.5 V, $V_I = V_{SS}$	—	—	–100	µA
C_I	Input capacitance		—	3.7	5	pF
C_O	Output capacitance		—	3.7	5	pF
Select Inputs A0, A1, A2, and $\overline{\text{RESET}}$						
V_{IL}	LOW level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH level input voltage		2.0	—	5.5	V
I_{LI}	Input leakage current		–1	—	1	µA

NOTES:
1. The total amount sunk by all I/Os must be limited to 100 mA and 25 mA per bit.
2. The total current sourced by all I/Os must be limited to 85 mA and 20 mA per bit.

AC SPECIFICATIONS

SYMBOL	PARAMETER	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNITS
		MIN	MAX	MIN	MAX	
f_{SCL}	Operating frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between STOP and START conditions	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time after (repeated) START condition	4.0	—	0.6	—	µs
$t_{SU;STA}$	Repeated START condition setup time	4.7	—	0.6	—	µs
$t_{SU;STO}$	Setup time for STOP condition	4.0	—	0.6	—	µs
$t_{HD;DAT}$	Data in hold time	0	—	0	—	ns
$t_{VD;ACK}$	Valid time for ACK condition[2]	—	1	—	0.9	µs
$t_{VD;DAT}$	Data out valid time[3]	—	1	—	0.9	µs
$t_{SU;DAT}$	Data setup time	250	—	100	—	ns
t_{LOW}	Clock LOW period	4.7	—	1.3	—	µs
t_{HIGH}	Clock HIGH period	4.0	—	0.6	—	µs
t_F	Clock/Data fall time	—	300	20 + 0.1 C_b[1]	300	ns
t_R	Clock/Data rise time	—	1000	20 + 0.1 C_b[1]	300	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
Port Timing						
t_{PV}	Output data valid I/O0	—	250	—	250	ns
t_{PV}	Output data valid I/O1 – I/O7	—	200	—	200	ns
t_{PS}	Input data setup time	0	—	0	—	ns
t_{PH}	Input data hold time	200	—	200	—	ns
Reset						
t_W	Reset pulse width	4	—	4	—	ns
t_{REC}	Reset recovery time	0	—	0	—	ns
t_{RESET}	Time to reset	400	—	400	—	ns

NOTES:
1. C_b = total capacitance of one bus line in pF.
2. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL low to SDA (out) low.
3. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL low.

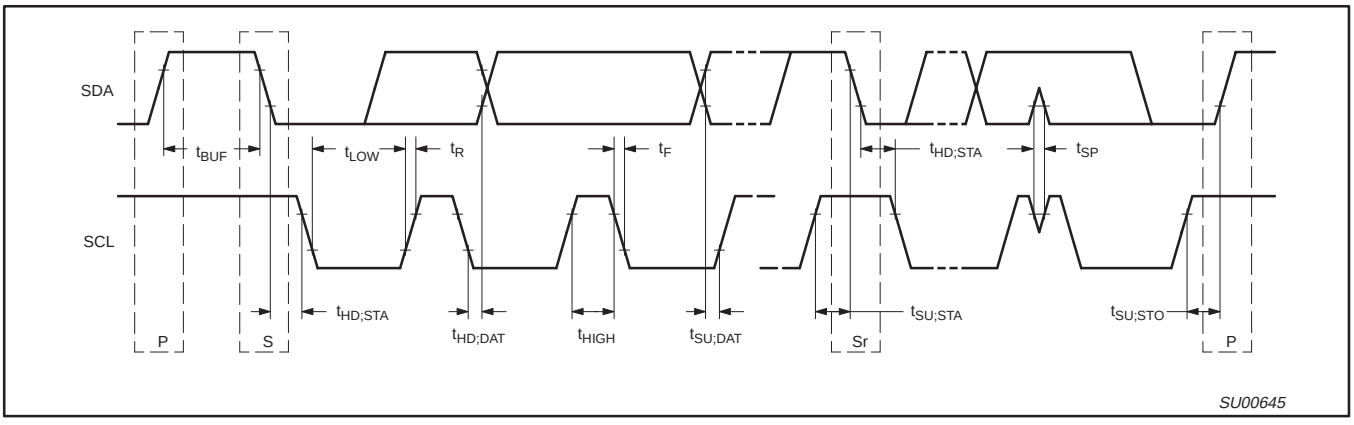
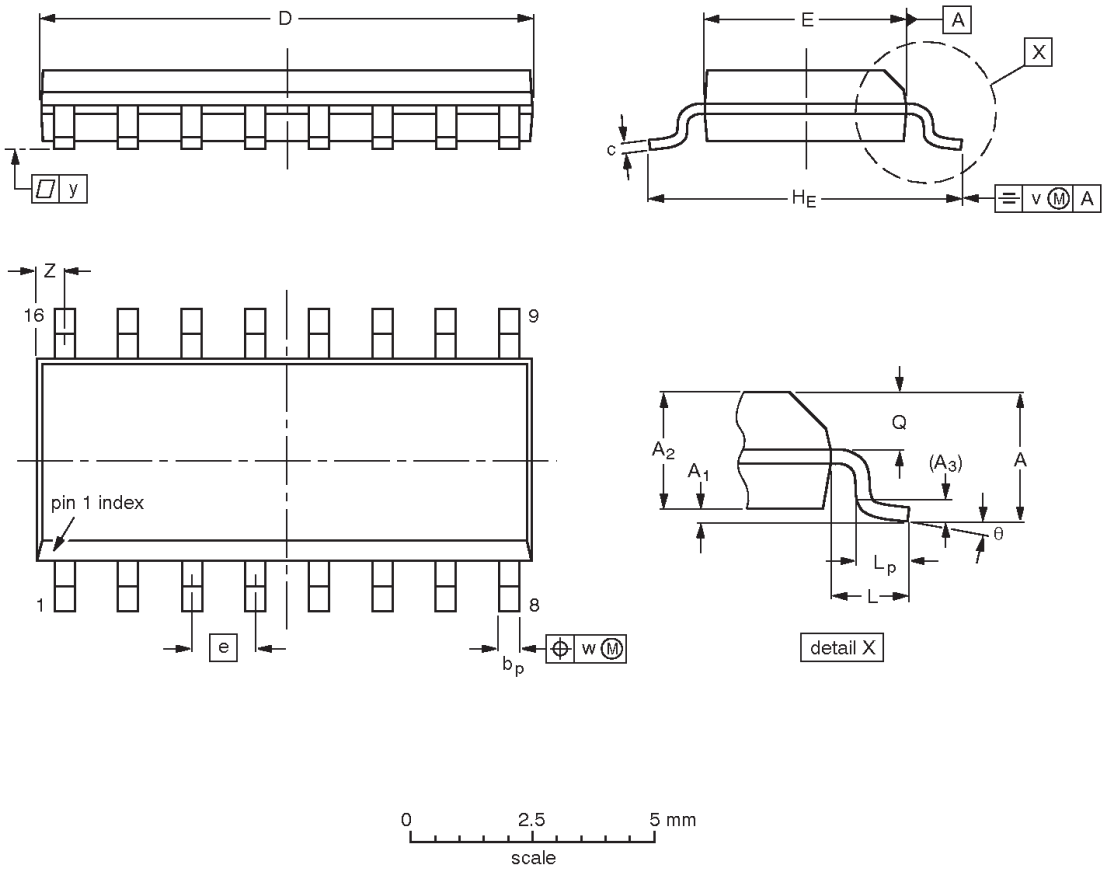


Figure 17. Definition of timing on the I²C-bus

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

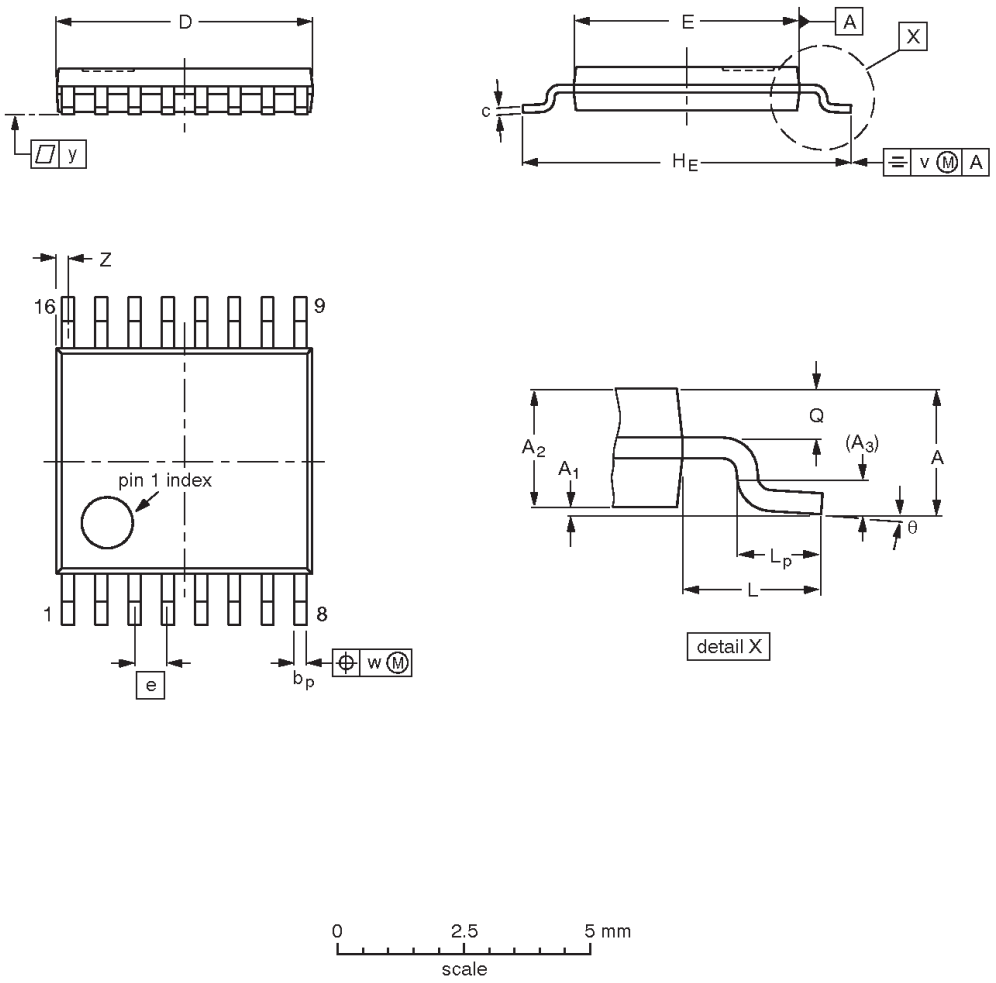
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				~~97-05-22~~ 99-12-27

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~95-04-04~~ 99-12-27

8-bit I²C and SMBus I/0 port with reset PCA9557

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Date of release: 12-01

Document order number: 9397 750 09217

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