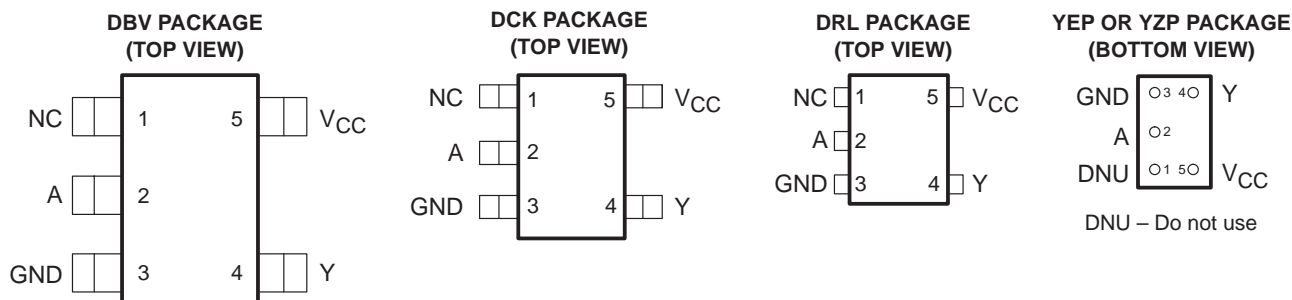


SN74AUP1G17 LOW-POWER SINGLE SCHMITT-TRIGGER BUFFER

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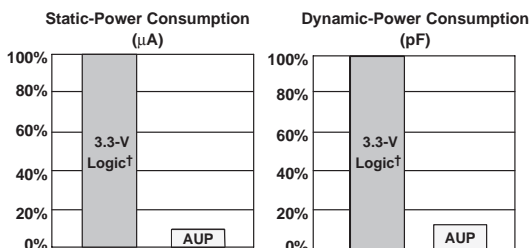
- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Low Static-Power Consumption; $I_{CC} = 0.9 \mu\text{A Max}$
- Low Dynamic-Power Consumption; $C_{pd} = 4.4 \text{ pF Typ at } 3.3 \text{ V}$
- Low Input Capacitance; $C_i = 1.5 \text{ pF Typ}$
- Low Noise – Overshoot and Undershoot <10% of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Includes Schmitt-Trigger Inputs
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 5.1 \text{ ns Max at } 3.3 \text{ V}$
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- ESD Protection Exceeds $\pm 5000 \text{ V}$ With Human-Body Model



See mechanical drawings for dimensions.

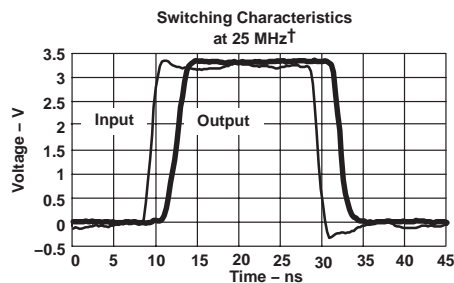
description/ordering information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figures 1 and 2).



† Single, dual, and triple gates

Figure 1. AUP–The Lowest-Power Family



† AUP1G08 data at $C_L = 15 \text{ pF}$

Figure 2. Excellent Signal Integrity



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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description/ordering information (continued)

This device functions as an independent gate with Schmitt-trigger inputs, which allows for slow input transition and better switching-noise immunity at the input.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74AUP1G17YEPR	___H7_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74AUP1G17YZPR	
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G17DBVR	H17_
		Reel of 250	SN74AUP1G17DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G17DCKR	H7_
		Reel of 250	SN74AUP1G17DCKT	
SOT (SOT-553) – DRL	Reel of 4000	SN74AUP1G17DRLR	H7_	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 4.6 V
Output voltage range in the high or low state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±20 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package	206°C/W
DCK package	252°C/W
DRL package	142°C/W
YEP/YZP package	132°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0.8	3.6	V
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}^\ddagger	High-level output current	$V_{CC} = 0.8$ V	–20	mA
		$V_{CC} = 1.1$ V	–1.1	
		$V_{CC} = 1.4$ V	–1.7	
		$V_{CC} = 1.65$	–1.9	
		$V_{CC} = 2.3$ V	–3.1	
		$V_{CC} = 3$ V	–4	
I_{OL}^\ddagger	Low-level output current	$V_{CC} = 0.8$ V	20	mA
		$V_{CC} = 1.1$ V	1.1	
		$V_{CC} = 1.4$ V	1.7	
		$V_{CC} = 1.65$ V	1.9	
		$V_{CC} = 2.3$ V	3.1	
		$V_{CC} = 3$ V	4	
T_A	Operating free-air temperature	–40	85	°C

‡ Defined by the signal-integrity requirements and design-goal priorities

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		T _A = -40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	
V _{T+} Positive-going input threshold voltage		0.8 V	0.3	0.6	0.3	0.6	V
		1.1 V	0.53	0.9	0.53	0.9	
		1.4 V	0.74	1.11	0.74	1.11	
		1.65 V	0.91	1.29	0.91	1.29	
		2.3 V	1.37	1.77	1.37	1.77	
		3 V	1.88	2.29	1.88	2.29	
V _{T-} Negative-going input threshold voltage		0.8 V	0.1	0.6	0.1	0.6	V
		1.1 V	0.26	0.65	0.26	0.65	
		1.4 V	0.39	0.75	0.39	0.75	
		1.65 V	0.47	0.84	0.47	0.84	
		2.3 V	0.69	1.04	0.69	1.04	
		3 V	0.88	1.24	0.88	1.24	
ΔV _T Hysteresis (V _{T+} - V _{T-})		0.8 V	0.07	0.5	0.07	0.5	V
		1.1 V	0.08	0.46	0.08	0.46	
		1.4 V	0.18	0.56	0.18	0.56	
		1.65 V	0.27	0.66	0.27	0.66	
		2.3 V	0.53	0.92	0.53	0.92	
		3 V	0.79	1.31	0.79	1.31	
V _{OH}	I _{OH} = -20 μA	0.8 V to 3.6 V	V _{CC} - 0.1		V _{CC} - 0.1		V
	I _{OH} = -1.1 mA	1.1 V	0.75 × V _{CC}		0.7 × V _{CC}		
	I _{OH} = -1.7 mA	1.4 V	1.11		1.03		
	I _{OH} = -1.9 mA	1.65 V	1.32		1.3		
	I _{OH} = -2.3 mA	2.3 V	2.05		1.97		
	I _{OH} = -3.1 mA		1.9		1.85		
	I _{OH} = -2.7 mA	3 V	2.72		2.67		
	I _{OH} = -4 mA		2.6		2.55		
V _{OL}	I _{OL} = 20 μA	0.8 V to 3.6 V	0.1		0.1		V
	I _{OL} = 1.1 mA	1.1 V	0.3 × V _{CC}		0.3 × V _{CC}		
	I _{OL} = 1.7 mA	1.4 V	0.31		0.37		
	I _{OL} = 1.9 mA	1.65 V	0.31		0.35		
	I _{OL} = 2.3 mA	2.3 V	0.31		0.33		
	I _{OL} = 3.1 mA		0.44		0.45		
	I _{OL} = 2.7 mA	3 V	0.31		0.33		
	I _{OL} = 4 mA		0.44		0.45		
I _I	A input	V _I = GND to 3.6 V	0 V to 3.6 V		0.1		μA
I _{off}		V _I or V _O = 0 V to 3.6 V	0 V		0.2		μA
ΔI _{off}		V _I or V _O = 0 V to 3.6 V	0 V to 0.2 V		0.2		μA
I _{CC}		V _I = GND or (V _{CC} to 3.6 V), I _O = 0	0.8 V to 3.6 V		0.5		μA
ΔI _{CC}		V _I = V _{CC} - 0.6 V, I _O = 0	3.3 V		40		μA



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LOW-POWER SINGLE SCHMITT-TRIGGER BUFFER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	V _{CC}	TYP	UNIT
C _i	V _I = V _{CC} or GND	0 V	1.5	pF
		3.6 V	1.5	
C _o	V _O = GND	0 V	2.5	pF

switching characteristics over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			T _A = -40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A	Y	0.8 V	22.7					ns
			1.2 V ± 0.1 V	6.3	8	12.8	3.9	14.6	
			1.5 V ± 0.1 V	4.6	5.8	8.4	2.8	10	
			1.8 V ± 0.15 V	3.9	4.8	7.2	2.4	8.1	
			2.5 V ± 0.2 V	3.1	3.6	5.1	2	6.1	
			3.3 V ± 0.3 V	2.7	3	4.4	1.9	5.1	

switching characteristics over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			T _A = -40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A	Y	0.8 V	25.1					ns
			1.2 V ± 0.1 V	7.1	9.1	13.8	4.7	15.6	
			1.5 V ± 0.1 V	5.2	6.5	9.4	3.4	11	
			1.8 V ± 0.15 V	4.5	5.4	8	2.9	9	
			2.5 V ± 0.2 V	3.5	4.2	5.7	2.4	6.8	
			3.3 V ± 0.3 V	3.1	3.5	4.9	2.2	5.7	

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			T _A = -40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A	Y	0.8 V	27.6					ns
			1.2 V ± 0.1 V	7.8	10.1	14.8	5.3	16.7	
			1.5 V ± 0.1 V	5.8	7.4	10.3	3.9	12	
			1.8 V ± 0.15 V	5	6.1	8.8	3.4	10	
			2.5 V ± 0.2 V	4	4.7	6.4	2.8	7.5	
			3.3 V ± 0.3 V	3.5	4.1	5.4	2.6	6.2	



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switching characteristics over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figures 3 and 4)

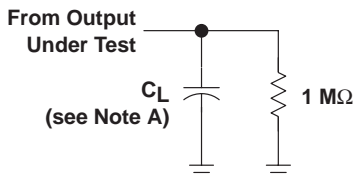
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V	35.1					ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	10	13.1	18.1	7.5	19.8	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	7.4	9.6	12.9	5.6	14.9	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	6.4	7.9	11	4.8	12.4	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	5.2	6.1	7.9	4	9.3	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	4.6	5.3	6.7	3.6	7.7	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$f = 10 \text{ MHz}$	0.8 V	4	pF
		$1.2 \text{ V} \pm 0.1 \text{ V}$	4	
		$1.5 \text{ V} \pm 0.1 \text{ V}$	4	
		$1.8 \text{ V} \pm 0.15 \text{ V}$	4	
		$2.5 \text{ V} \pm 0.2 \text{ V}$	4.2	
		$3.3 \text{ V} \pm 0.3 \text{ V}$	4.4	

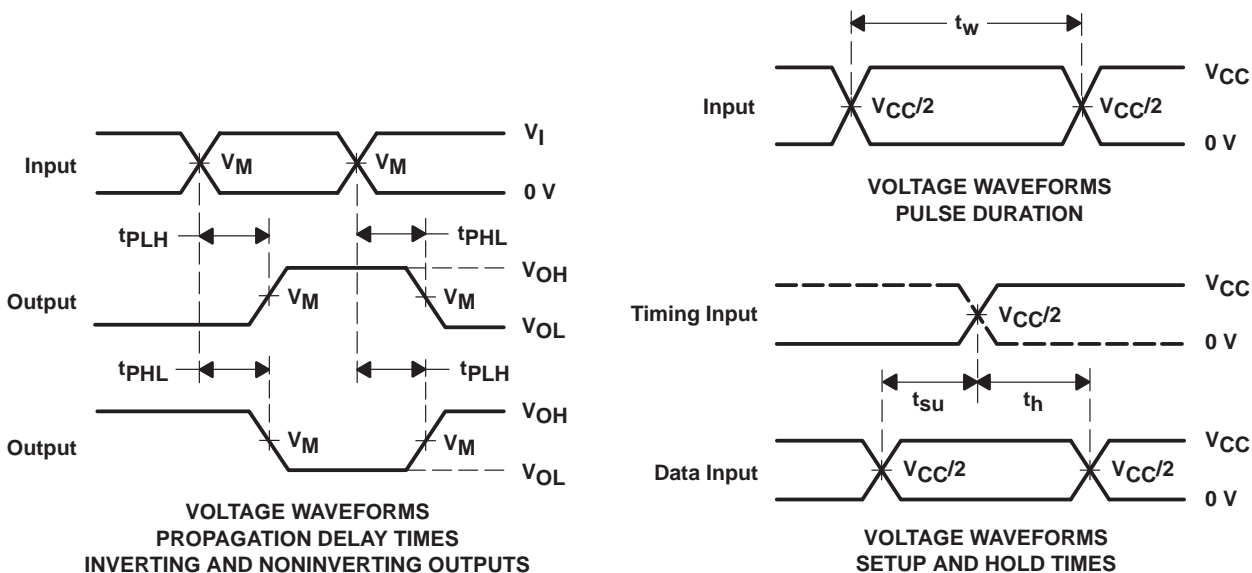


PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)



LOAD CIRCUIT

	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



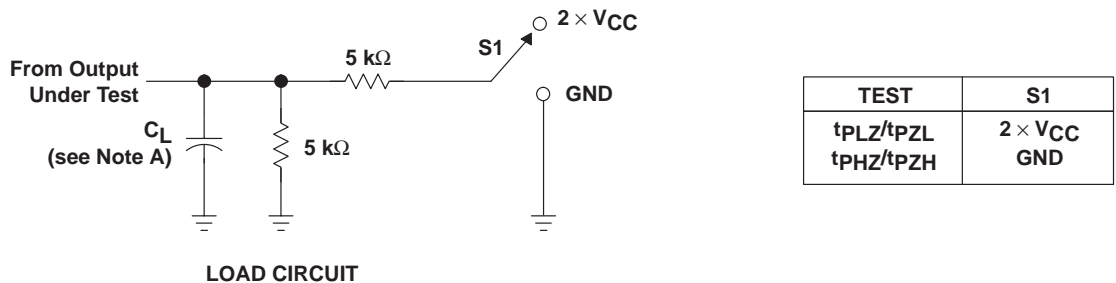
- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r/t_f = 3\text{ ns}$.
 C. The outputs are measured one at a time, with one transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .
 E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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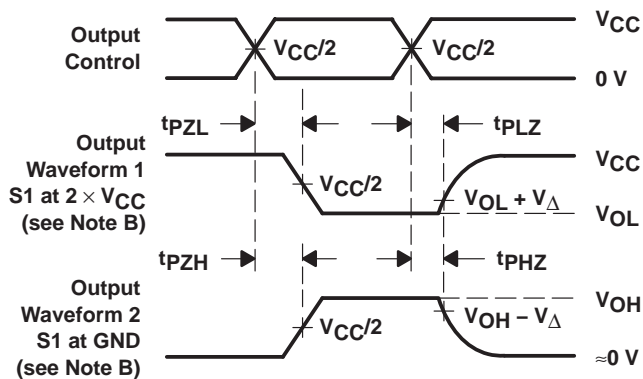
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PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AUP1G17DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G17DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G17DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G17DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G17DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G17DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G17DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G17DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G17DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G17DRLR	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G17DRLRG4	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G17YEPR	NRND	WCSP	YEP	5	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74AUP1G17YZPR	ACTIVE	WCSP	YZP	5	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DBV (R-PDSO-G5)

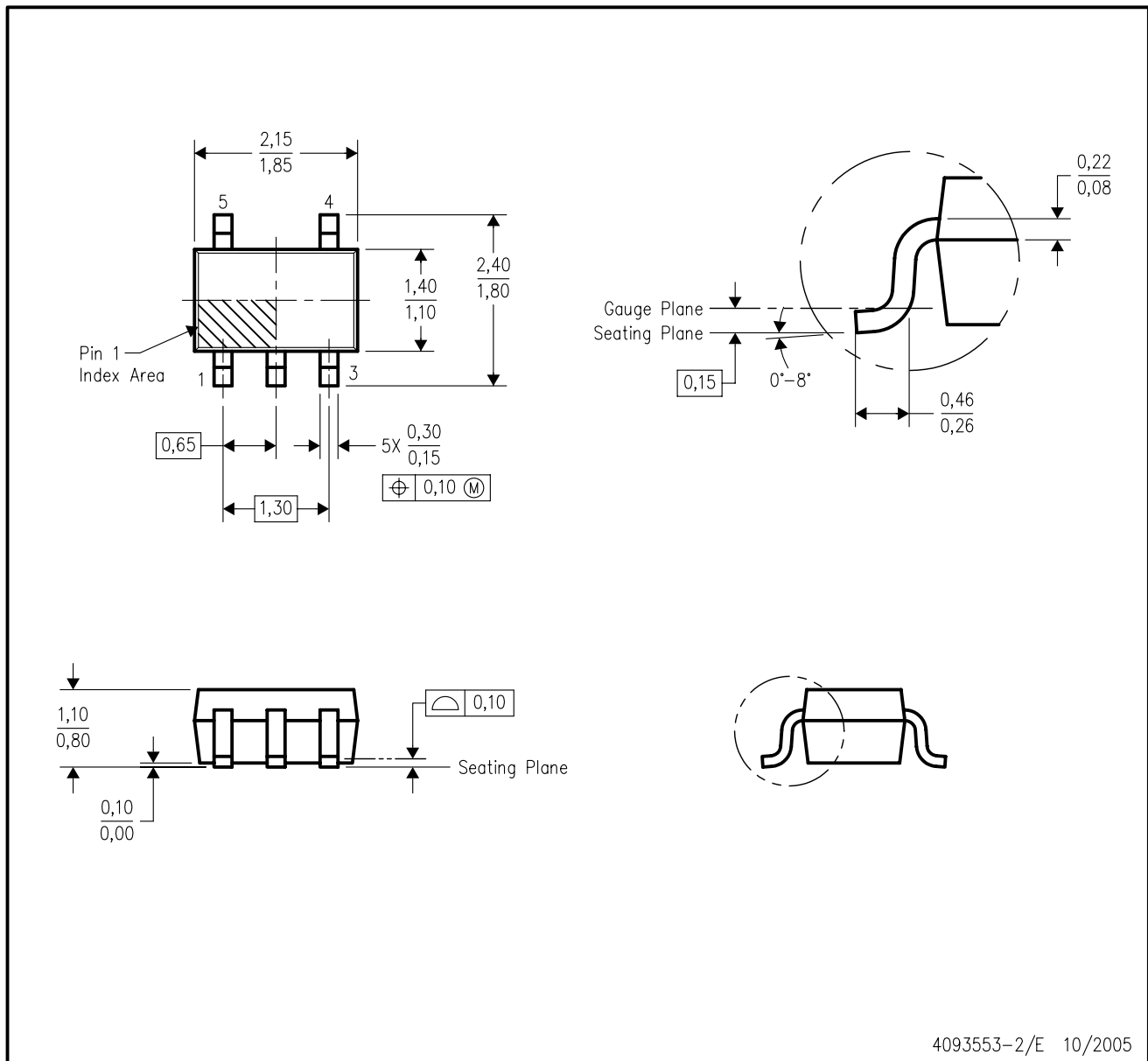
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DCK (R-PDSO-G5)

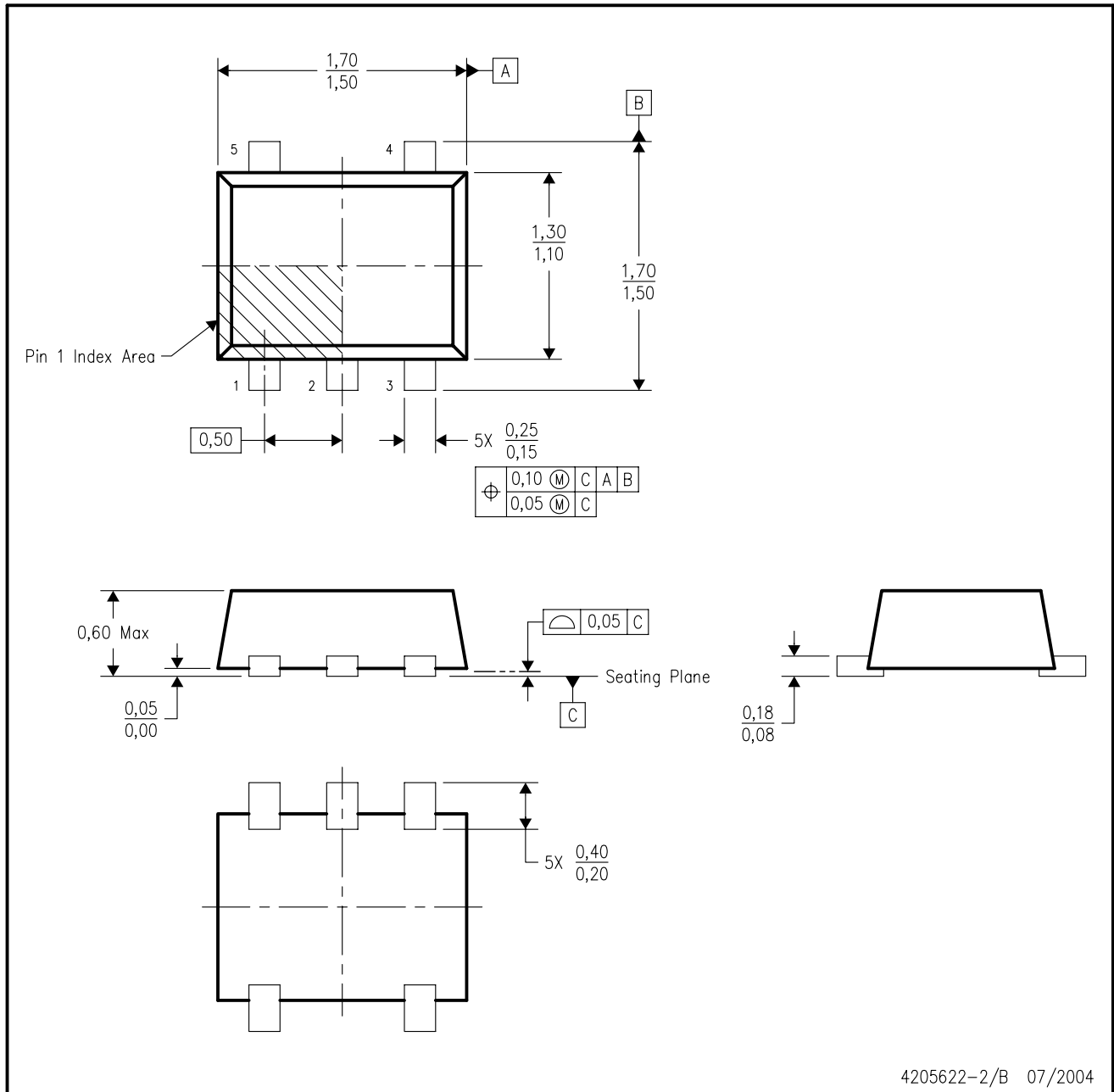
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
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 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

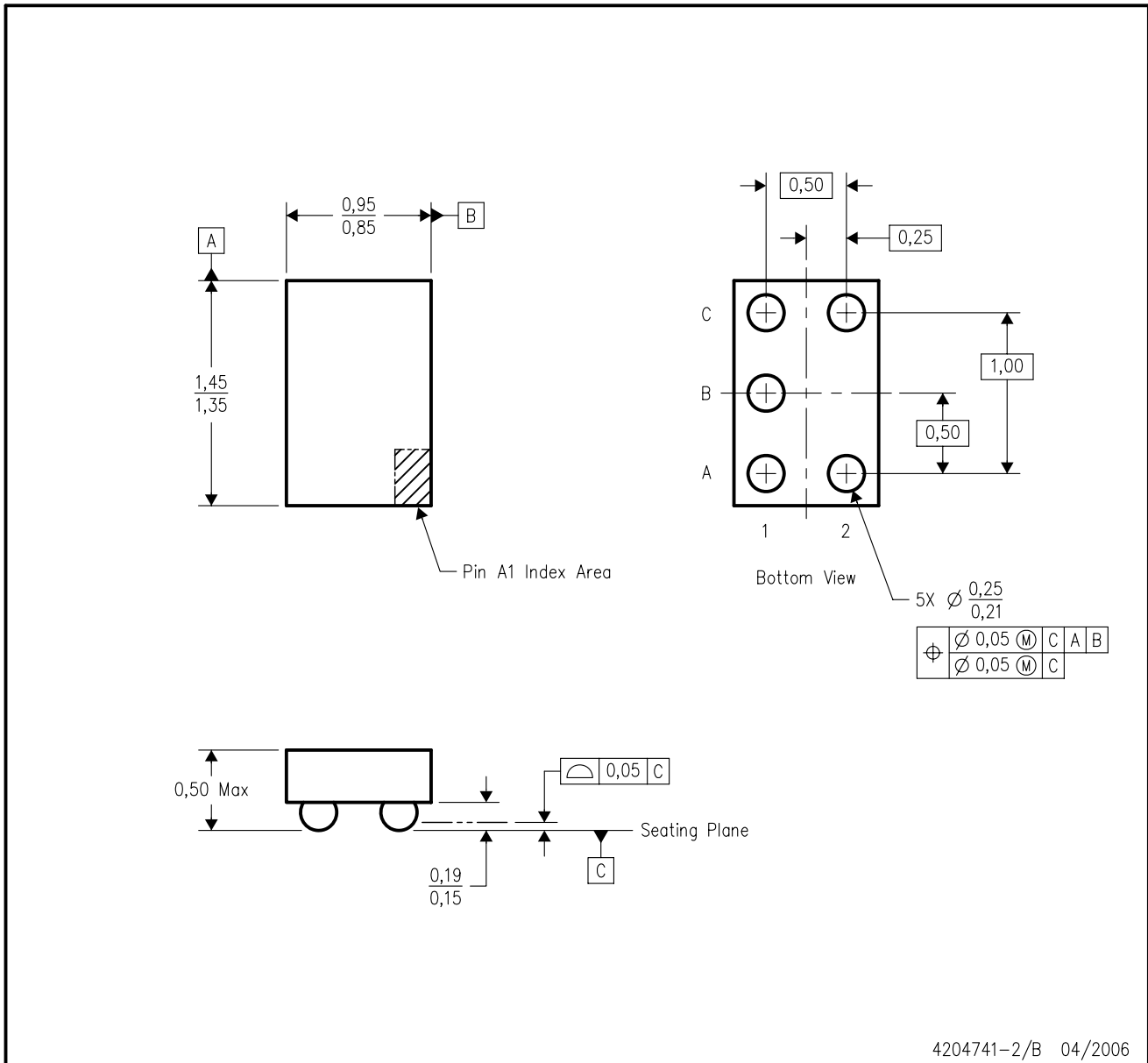


4205622-2/B 07/2004

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. JEDEC package registration is pending.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



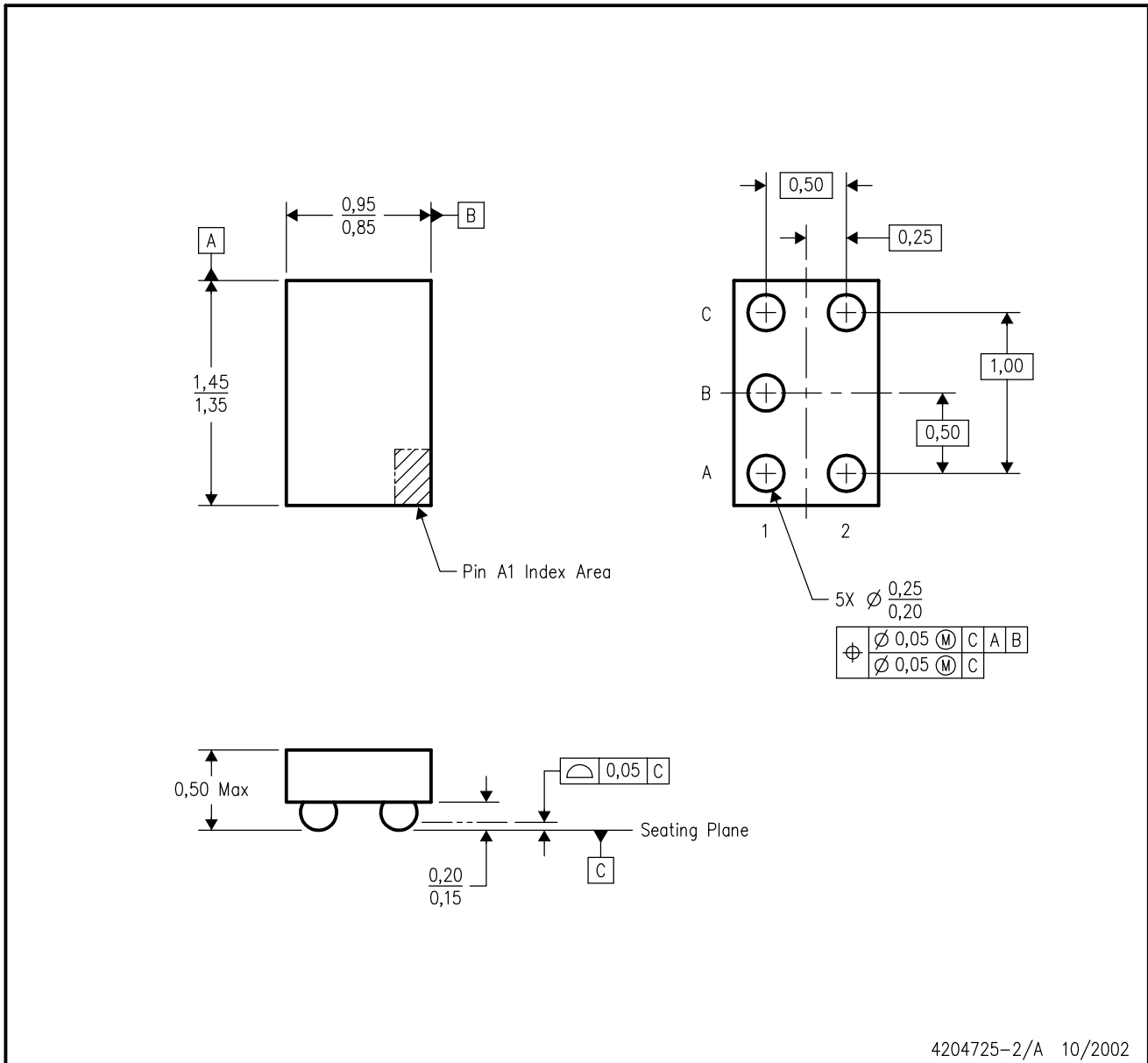
4204741-2/B 04/2006

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead-free.

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