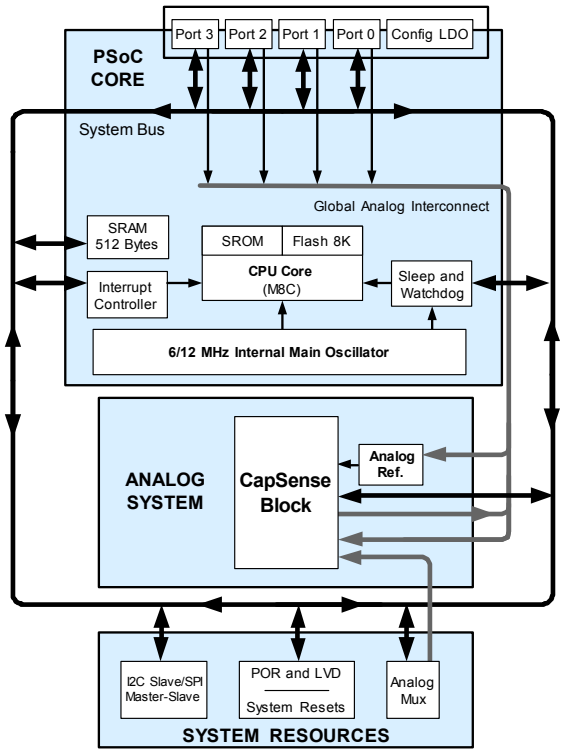
CY8C20234, CY8C20334
CY8C20434, CY8C20534

PSoC® Programmable System-0n-Chip™

Features

- Low Power CapSense™ Block
  - Configurable Capacitive Sensing Elements
  - Supports Combination of CapSense Buttons, Sliders, Touch-pads, and Proximity Sensors
- Powerful Harvard Architecture Processor
  - M8C Processor Speeds Running up to 12 MHz
  - Low Power at High Speed
  - 2.4V to 5.25V Operating Voltage
  - Industrial Temperature Range: -40°C to +85°C
- Flexible On-Chip Memory
  - 8K Flash Program Storage 50,000 Erase/Write Cycles
  - 512 Bytes SRAM Data Storage
  - Partial Flash Updates
  - Flexible Protection Modes
  - Interrupt Controller
  - In-System Serial Programming (ISSP)
- Complete Development Tools
  - Free Development Tool (PSoC Designer™)
  - Full Featured, In-Circuit Emulator, and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128K Trace Memory
- Precision, Programmable Clocking
  - Internal ±5.0% 6/12 MHz Main Oscillator
  - Internal Low Speed Oscillator at 32 kHz for Watchdog and Sleep
- Programmable Pin Configurations
  - Pull Up, High Z, Open Drain, and CMOS Drive Modes on All GPIO
  - Up to 28 Analog Inputs on GPIO
  - Configurable Inputs on All GPIO
  - Selectable, Regulated Digital I/O on Port 1
    - 3.0V, 20 mA Total Port 1 Source Current
    - 5 mA Strong Drive Mode on Port 1 Versatile Analog Mux
  - Common Internal Analog Bus
  - Simultaneous Connection of I/O Combinations
  - Comparator Noise Immunity
  - Low Dropout Voltage Regulator for the Analog Array
- Additional System Resources
  - Configurable Communication Speeds
    - I^2C: Selectable to 50 kHz, 100 kHz, or 400 kHz
    - SPI: Configurable between 46.9 kHz and 3 MHz
  - I^2C Slave
  - SPI Master and SPI Slave
  - Watchdog and Sleep Timers
  - Internal Voltage Reference
  - Integrated Supervisory Circuit

Logic Block Diagram



PSoC® Functional Overview

The PSoCfamily consists of many *Programmable System-on-Chips with On-Chip Controller* devices. These devices are designed to replace multiple traditional MCU based system components with one low cost single chip programmable component. A PSoC device includes configurable analog and digital blocks and programmable interconnect. This architecture enables the user to create customized peripheral configurations to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture for this device family, as shown in Figure 1, consists of three main areas: the Core, the System Resources, and the CapSense Analog System. A common versatile bus enables connection between I/O and the analog system. Each CY8C20x34 PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 28 general purpose IO (GPIO) are also included. The GPIO provide access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, IMO (Internal Main Oscillator), and ILO (Internal Low speed Oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a two MIPS, 8-bit Harvard architecture microprocessor.

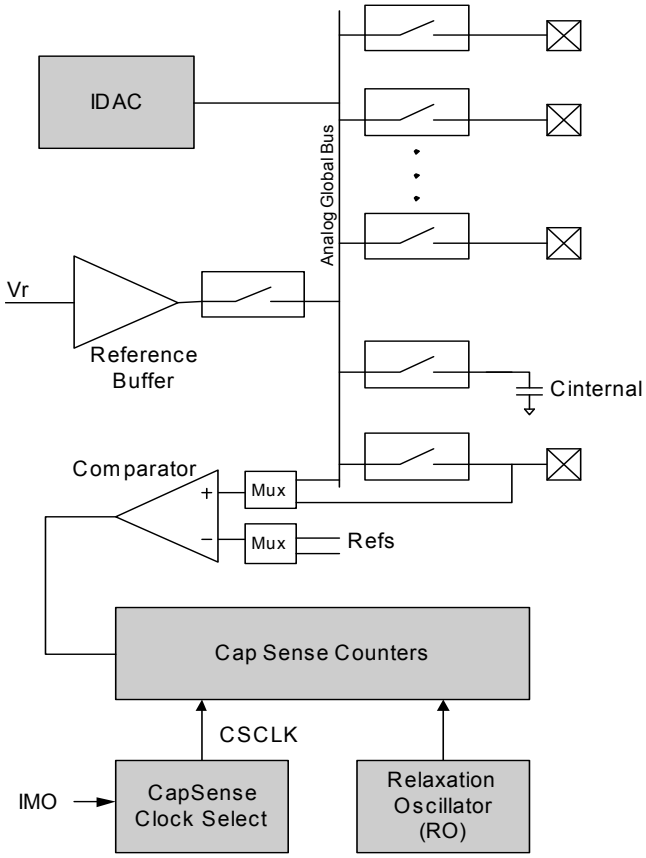
System Resources provide additional capability such as a configurable I^2C slave or SPI master-slave communication interface and various system resets supported by the M8C.

The Analog System consists of the CapSense PSoC block and an internal 1.8V analog reference. Together they support capacitive sensing of up to 28 inputs.

CapSense Analog System

The Analog System contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins is completed quickly and easily across multiple ports.

Figure 1. Analog System Block Diagram



Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces such as sliders and touch pads
- Chip-wide mux that enables analog input from any I/O pin
- Crosspoint connection between any I/O pin combinations

When designing capacitive sensing applications, refer to the latest signal-to-noise signal level requirements Application Notes, found under http://www.cypress.com >> DESIGN RESOURCES >> Application Notes. In general, unless otherwise noted in the relevant Application Notes, the minimum signal-to-noise ratio (SNR) requirement for CapSense applications is 5:1.

Additional System Resources

System Resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. Brief statements describing the merits of each system resource are presented below.

- The I^2C slave or SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires run at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- Low Voltage Detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.8V reference provides an absolute reference for capacitive sensing.
- The 5V maximum input, 3V fixed output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.

Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming information, see the PSoC® Programmable System-on-Chip Technical Reference Manual for CY8C28xxx PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at www.cypress.com/psoc.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

Cypros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

PSoC Designer Software Subsystems

System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC Mixed-Signal Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select components
2. Configure components
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I^2C-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view, the components are called “user modules”. User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog to digital converter (ADC) to convert the potentiometer’s output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Table 1 lists the acronyms that are used in this document.

Table 1. Acronyms Used

Acronym	Description
AC	Alternating Current
API	Application Programming Interface
CPU	Central Processing Unit
DC	Direct Current
GPIO	General Purpose IO
GUI	Graphical User Interface
ICE	In-Circuit Emulator
ILO	Internal Low Speed Oscillator
IMO	Internal Main Oscillator
I/O	Input Or Output
LSb	Least Significant Bit
LVD	Low Voltage Detect
MSb	Most Significant Bit
POR	Power On Reset
PPOR	Precision Power On Reset
PSoC®	Programmable System-on-Chip™
SLIMO	Slow IMO
SRAM	Static Random Access Memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 7 on page 14 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers are also represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b or 01000011b). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimals.

Pin Information

This section describes, lists, and illustrates the CY8C20234, CY8C20334, CY8C20434, and CY8C20534 PSoC device pins and pinout configurations.

The CY8C20x34 PSoC device is available in a variety of packages that are listed and shown in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, Vss, Vdd, and XRES are not capable of Digital I/O.

16-Pin Part Pinout

Figure 2. CY8C20234 16-Pin PSoC Device

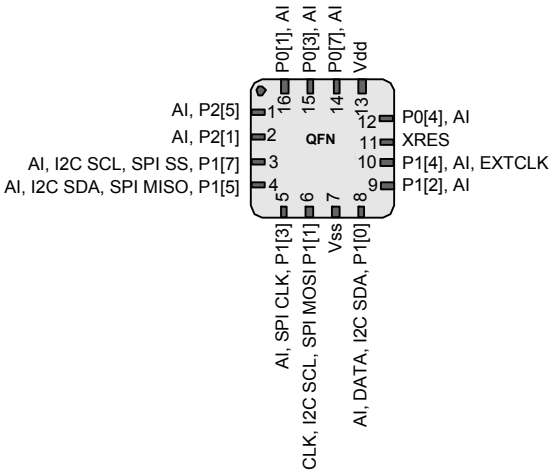


Table 2. Pin Definitions - CY8C20234 16-Pin (QFN)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[1]	
3	IOH	I	P1[7]	I^2C SCL, SPI SS
4	IOH	I	P1[5]	I^2C SDA, SPI MISO
5	IOH	I	P1[3]	SPI CLK
6	IOH	I	P1[1]	CLK[1], I^2C SCL, SPI MOSI
7	Power		Vss	Ground Connection
8	IOH	I	P1[0]	DATA[1], I^2C SDA
9	IOH	I	P1[2]	
10	IOH	I	P1[4]	Optional External Clock Input (EXTCLK)
11	Input		XRES	Active High External Reset with Internal Pull Down
12	I/O	I	P0[4]	
13	Power		Vdd	Supply Voltage
14	I/O	I	P0[7]	
15	I/O	I	P0[3]	Integrating Input
16	I/O	I	P0[1]	

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Note
1. These are the ISSP pins, that are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

24-Pin Part Pinout

Figure 3. CY8C20334 24-Pin PSoC Device

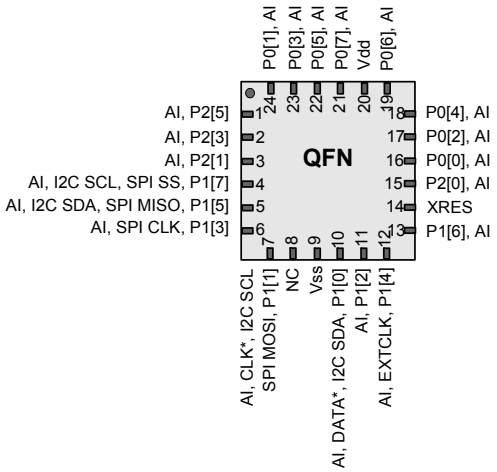


Table 3. Pin Definitions - CY8C20334 24-Pin (QFN) [2]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	IOH	I	P1[7]	I^2C SCL, SPI SS
5	IOH	I	P1[5]	I^2C SDA, SPI MISO
6	IOH	I	P1[3]	SPI CLK
7	IOH	I	P1[1]	CLK[1], I^2C SCL, SPI MOSI
8			NC	No Connection
9	Power		Vss	Ground Connection
10	IOH	I	P1[0]	DATA[1], I^2C SDA
11	IOH	I	P1[2]	
12	IOH	I	P1[4]	Optional External Clock Input (EXTCLK)
13	IOH	I	P1[6]	
14	Input		XRES	Active High External Reset with Internal Pull Down
15	I/O	I	P2[0]	
16	I/O	I	P0[0]	
17	I/O	I	P0[2]	
18	I/O	I	P0[4]	
19	I/O	I	P0[6]	Analog Bypass
20	Power		Vdd	Supply Voltage
21	I/O	I	P0[7]	
22	I/O	I	P0[5]	
23	I/O	I	P0[3]	Integrating Input
24	I/O	I	P0[1]	
CP	Power		Vss	Center Pad is connected to Ground

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Note
2. The center pad on the QFN package is connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.

28-Pin Part Pinout

Figure 4. CY8C20534 28-Pin PSoC Device

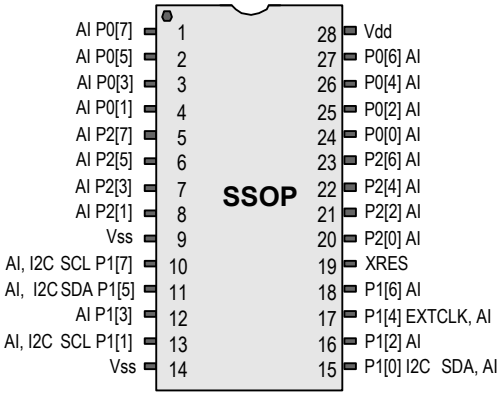


Table 4. Pin Definitions - CY8C20534 28-Pin (SSOP)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog Column Mux Input
2	I/O	I	P0[5]	Analog Column Mux Input and Column Output
3	I/O	I	P0[3]	Analog Column Mux Input and Column Output, Integrating Input
4	I/O	I	P0[1]	Analog Column Mux Input, Integrating Input
5	I/O	I	P2[7]	
6	I/O	I	P2[5]	
7	I/O	I	P2[3]	Direct Switched Capacitor Block Input
8	I/O	I	P2[1]	Direct Switched Capacitor Block Input
9	Power		Vss	Ground Connection
10	I/O	I	P1[7]	I2C Serial Clock (SCL)
11	I/O	I	P1[5]	I2C Serial Data (SDA)
12	I/O	I	P1[3]	
13	I/O	I	P1[1]	I2C Serial Clock (SCL), ISSP-SCLK[1]
14	Power		Vss	Ground Connection
15	I/O	I	P1[0]	I2C Serial Data (SDA), ISSP-SDATA[1]
16	I/O	I	P1[2]	
17	I/O	I	P1[4]	Optional External Clock Input (EXTCLK)
18	I/O	I	P1[6]	
19	Input		XRES	Active High External Reset with Internal Pull Down
20	I/O	I	P2[0]	Direct Switched Capacitor Block Input
21	I/O	I	P2[2]	Direct Switched Capacitor Block Input
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	I/O	I	P0[0]	Analog Column Mux Input
25	I/O	I	P0[2]	Analog Column Mux Input
26	I/O	I	P0[4]	Analog Column Mux Input
27	I/O	I	P0[6]	Analog Column Mux Input
28	Power		Vdd	Supply Voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

32-Pin Part Pinout

Figure 5. CY8C20434 32-Pin PSoC Device

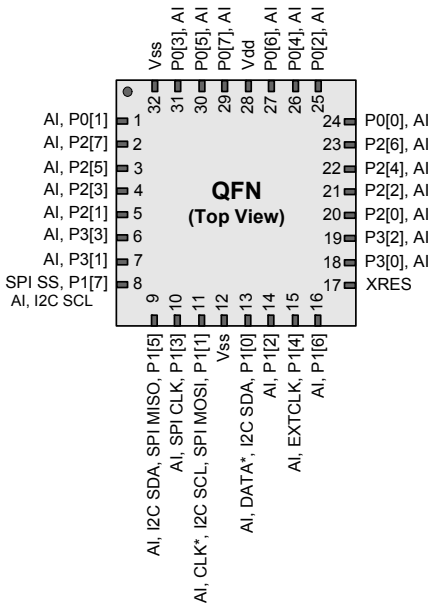


Table 5. Pin Definitions - CY8C20434 32-Pin (QFN) [2]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[1]	
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	
4	I/O	I	P2[3]	
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOH	I	P1[7]	I^2C SCL, SPI SS
9	IOH	I	P1[5]	I^2C SDA, SPI MISO
10	IOH	I	P1[3]	SPI CLK
11	IOH	I	P1[1]	CLK[1], I^2C SCL, SPI MOSI
12	Power		Vss	Ground Connection
13	IOH	I	P1[0]	DATA[1], I^2C SDA
14	IOH	I	P1[2]	
15	IOH	I	P1[4]	Optional External Clock Input (EXTCLK)
16	IOH	I	P1[6]	
17	Input		XRES	Active High External Reset With Internal Pull Down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	

Table 5. Pin Definitions - CY8C20434 32-Pin (QFN) [2] (continued)

Pin No.	Type		Name	Description
	Digital	Analog		
23	I/O	I	P2[6]	
24	I/O	I	P0[0]	
25	I/O	I	P0[2]	
26	I/O	I	P0[4]	
27	I/O	I	P0[6]	Analog Bypass
28	Power		Vdd	Supply Voltage
29	I/O	I	P0[7]	
30	I/O	I	P0[5]	
31	I/O	I	P0[3]	Integrating Input
32	Power		Vss	Ground Connection
CP	Power		Vss	Center Pad Is Connected to Ground

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

48-Pin OCD Part Pinout

The 48-Pin QFN part table and pin diagram is for the CY8C20000 On-Chip Debug (OCD) PSoC device. This part is only used for in-circuit debugging. It is NOT available for production.

Figure 6. CY8C20000 48-Pin OCD PSoC Device

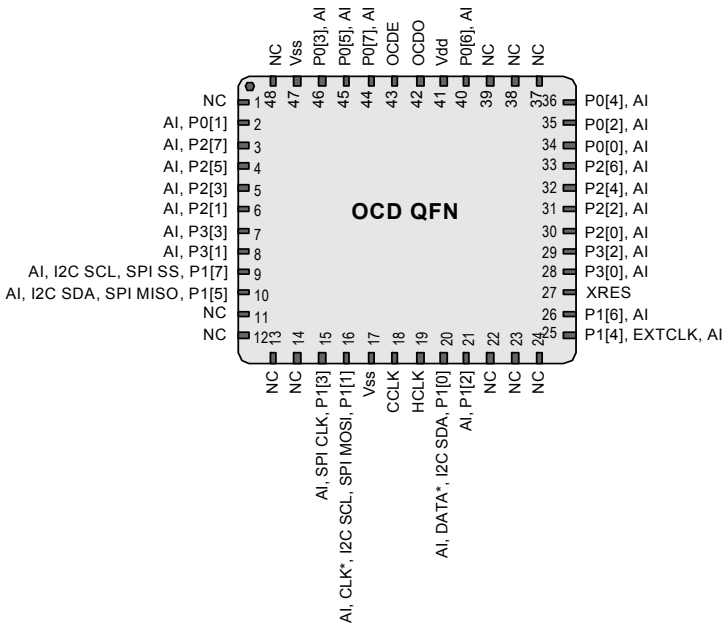


Table 6. Pin Definitions - CY8C20000 48-Pin OCD (QFN) [2]

Pin No.	Digital	Analog	Name	Description
1			NC	No Connection
2	I/O	I	P0[1]	
3	I/O	I	P2[7]	
4	I/O	I	P2[5]	
5	I/O	I	P2[3]	
6	I/O	I	P2[1]	
7	I/O	I	P3[3]	
8	I/O	I	P3[1]	
9	IOH	I	P1[7]	I^2C SCL, SPI SS
10	IOH	I	P1[5]	I^2C SDA, SPI MISO
11	I/O	I	P0[1]	
12			NC	No Connection
13			NC	No Connection
14			NC	No Connection
15			NC	No Connection
16	IOH	I	P1[3]	SPI CLK
17	IOH	I	P1[1]	CLK[1], I^2C SCL, SPI MOSI
18	Power		Vss	Ground Connection

Table 6. Pin Definitions - CY8C20000 48-Pin OCD (QFN) [2] (continued)

Pin No.	Digital	Analog	Name	Description
19			CCLK	OCD CPU Clock Output
20			HCLK	OCD High Speed Clock Output
21	IOH	I	P1[0]	DATA[1], I^2C SDA
22	IOH	I	P1[2]	
23			NC	No Connection
24			NC	No Connection
25			NC	No Connection
26	IOH	I	P1[4]	Optional External Clock Input (EXTCLK)
27	IOH	I	P1[6]	
28	Input		XRES	Active High External Reset with Internal Pull Down
29	I/O	I	P3[0]	
30	I/O	I	P3[2]	
31	I/O	I	P2[0]	
32	I/O	I	P2[2]	
33	I/O	I	P2[4]	
34	I/O	I	P2[6]	
35	I/O	I	P0[0]	
36	I/O	I	P0[2]	
37			NC	No Connection
38			NC	No Connection
39			NC	No Connection
40	I/O	I	P0[6]	Analog Bypass
41	Power		Vdd	Supply Voltage
42			OCDO	OCD Odd Data Output
43			OCDE	OCD Even Data I/O
44	I/O	I	P0[7]	
45	I/O	I	P0[5]	
46	I/O	I	P0[3]	Integrating Input
47	Power		Vss	Ground Connection
48			NC	No Connection
CP	Power		Vss	Center Pad is connected to Ground

A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20234, CY8C20334, CY8C20434, and CY8C20534 PSoC devices. For the latest electrical specifications, check the most recent data sheet by visiting the web at http://www.cypress.com/psoc.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C as specified, except where mentioned.

Refer to Table 17 on page 20 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 7. Voltage versus CPU Frequency and IMO Frequency Trim Options

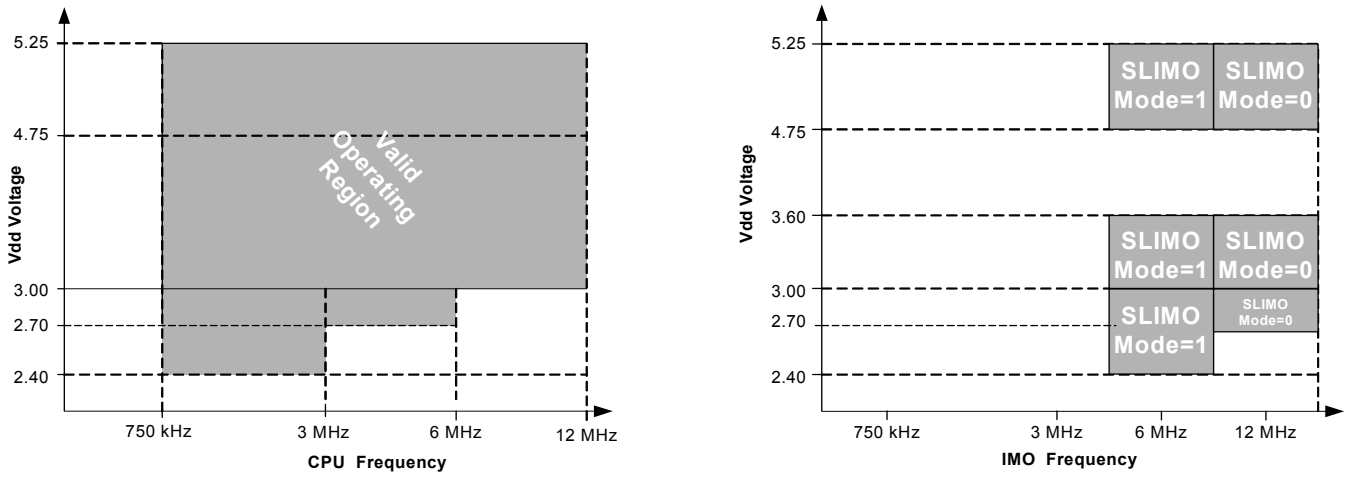


Table 7 lists the units of measure that are used in this section.

Table 7. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milliampere
fF	femto farad	ms	millisecond
Hz	hertz	mV	millivolts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	W	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	s	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrades reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up Current	–	–	200	mA	

Operating Temperature

Table 9. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 15 on page 18. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip Level Specifications

Table 10 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 10. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	2.40	–	5.25	V	See Table 15 on page 18.
I_{DD12}	Supply Current, IMO = 12 MHz	–	1.5	2.5	mA	Conditions are Vdd = 3.0V, T_A = 25°C, CPU = 12 MHz.
I_{DD6}	Supply Current, IMO = 6 MHz	–	1	1.5	mA	Conditions are Vdd = 3.0V, T_A = 25°C, CPU = 6 MHz
I_{SB27}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and Internal Slow Oscillator Active. Mid Temperature Range.	–	2.6	4.	µA	Vdd = 2.55V, 0°C ≤ T_A ≤ 40°C
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and Internal Slow Oscillator Active.	–	2.8	5	µA	Vdd = 3.3V, -40°C ≤ T_A ≤ 85°C

DC General Purpose IO Specifications

Unless otherwise noted, Table 11 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ TA ≤ 85°C, 3.0V to 3.6V and -40°C ≤ TA ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ TA ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C. These are for design guidance only.

Table 11. 5V and 3.3V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
V_{OH1}	High Output Voltage Port 0, 2, or 3 Pins	Vdd - 0.2	–	–	V	IOH ≤ 10 µA, Vdd ≥ 3.0V, maximum of 20 mA source current in all IOs.
V_{OH2}	High Output Voltage Port 0, 2, or 3 Pins	Vdd - 0.9	–	–	V	IOH = 1 mA, Vdd ≥ 3.0V, maximum of 20 mA source current in all IOs.
V_{OH3}	High Output Voltage Port 1 Pins with LDO Regulator Disabled	Vdd - 0.2	–	–	V	IOH < 10 µA, Vdd ≥ 3.0V, maximum of 10 mA source current in all IOs.
V_{OH4}	High Output Voltage Port 1 Pins with LDO Regulator Disabled	Vdd - 0.9	–	–	V	IOH = 5 mA, Vdd ≥ 3.0V, maximum of 20 mA source current in all IOs.
V_{OH5}	High Output Voltage Port 1 Pins with 3.0V LDO Regulator Enabled	2.7	3.0	3.3	V	IOH < 10 µA, Vdd ≥ 3.1V, maximum of 4 IOs all sourcing 5 mA.
V_{OH6}	High Output Voltage Port 1 Pins with 3.0V LDO Regulator Enabled	2.2	–	–	V	IOH = 5 mA, Vdd ≥ 3.1V, maximum of 20 mA source current in all IOs.
V_{OH7}	High Output Voltage Port 1 Pins with 2.4V LDO Regulator Enabled	2.1	2.4	2.7	V	IOH < 10 µA, Vdd ≥ 3.0V, maximum of 20 mA source current in all IOs.
V_{OH8}	High Output Voltage Port 1 Pins with 2.4V LDO Regulator Enabled	2.0	–	–	V	IOH < 200 µA, Vdd ≥ 3.0V, maximum of 20 mA source current in all IOs.
V_{OH9}	High Output Voltage Port 1 Pins with 1.8V LDO Regulator Enabled	1.6	1.8	2.0	V	IOH < 10 µA 3.0V ≤ Vdd ≤ 3.6V 0°C ≤ TA ≤ 85°C Maximum of 20 mA source current in all IOs.

Table 11. 5V and 3.3V DC GPIO Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OH10}	High Output Voltage Port 1 Pins with 1.8V LDO Regulator Enabled	1.5	–	–	V	IOH < 100 μA. 3.0V ≤ Vdd ≤ 3.6V. 0°C ≤ TA ≤ 85°C. Maximum of 20 mA source current in all IOs.
V_{OL}	Low Output Voltage	–	–	0.75	V	IOL = 20 mA, Vdd > 3.0V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).
V_{IL}	Input Low Voltage	–	–	0.8	V	3.6V ≤ Vdd ≤ 5.25V
V_{IH}	Input High Voltage	2.0	–		V	3.6V ≤ Vdd ≤ 5.25V
V_H	Input Hysteresis Voltage	–	140	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA
C_{IN}	Capacitive Load on Pins as Input	0.5	1.7	5	pF	Package and pin dependent Temperature = 25°C
C_{OUT}	Capacitive Load on Pins as Output	0.5	1.7	5	pF	Package and pin dependent Temperature = 25°C

Table 12. 2.7V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
V_{OH1}	High Output Voltage Port 1 Pins with LDO Regulator Disabled	Vdd - 0.2	–	–	V	IOH < 10 μA, maximum of 10 mA source current in all IOs.
V_{OH2}	High Output Voltage Port 1 Pins with LDO Regulator Disabled	Vdd - 0.5	–	–	V	IOH = 2 mA, maximum of 10 mA source current in all IOs.
V_{OL}	Low Output Voltage	–	–	0.75	V	IOL = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]).
V_{OLP1}	Low Output Voltage Port 1 Pins	–	–	0.4	V	IOL=5 mA Maximum of 50 mA sink current on even port pins (for example, P0[2] and P3[4]) and 50 mA sink current on odd port pins (for example, P0[3] and P2[5]). 2.4V ≤ Vdd < 3.6V
V_{IL}	Input Low Voltage	–	–	0.75	V	2.4V ≤ Vdd < 3.6V
V_{IH1}	Input High Voltage	1.4	–	–	V	2.4V ≤ Vdd < 2.7V
V_{IH2}	Input High Voltage	1.6	–	–	V	2.7V ≤ Vdd < 3.6V
V_H	Input Hysteresis Voltage	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA
C_{IN}	Capacitive Load on Pins as Input	0.5	1.7	5	pF	Package and pin dependent Temperature = 25°C
C_{OUT}	Capacitive Load on Pins as Output	0.5	1.7	5	pF	Package and pin dependent Temperature = 25°C

DC Analog Mux Bus Specifications

Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 13. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch Resistance to Common Analog Bus	–	–	400 800	W W	Vdd ≥ 2.7V 2.4V ≤ Vdd ≤ 2.7V

DC Low Power Comparator Specifications

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 14. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	Vdd – 1	V	
I_{SLPC}	LPC supply current	–	10	40	µA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

DC POR and LVD Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 15. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	Vdd Value for PPOR Trip					Vdd is greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.60	2.65	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	2.82	2.95	V	
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.39	2.45	2.51[3]	V	
V_{LVD1}	VM[2:0] = 001b	2.54	2.71	2.78[4]	V	
V_{LVD2}	VM[2:0] = 010b	2.75	2.92	2.99[5]	V	
V_{LVD3}	VM[2:0] = 011b	2.85	3.02	3.09	V	
V_{LVD4}	VM[2:0] = 100b	2.96	3.13	3.20	V	
V_{LVD5}	VM[2:0] = 101b	–	–	–	V	
V_{LVD6}	VM[2:0] = 110b	–	–	–	V	
V_{LVD7}	VM[2:0] = 111b	4.52	4.73	4.83	V	

Notes
3. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
4. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
5. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.

DC Programming Specifications

Table 16 lists the guaranteed minimum and maximum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ TA ≤ 85°C, 3.0V to 3.6V and -40°C ≤ TA ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ TA ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only. Flash Endurance and Retention specifications with the use of the EEPROM User Module are valid only within the range: 25°C +/-20C during the Flash Write operation. Reference the EEPROM User Module data sheet instructions for EEPROM Flash Write requirements outside of the 25°C +/-20°C temperature window.

Table 16. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations	2.70	–	–	V	
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd –1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[6]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Note
6. A maximum of 36 x 50,000 block endurance cycles is allowed. This is balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

AC Electrical Characteristics

AC Chip Level Specifications

Table 17, Table 18, and Table 19 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 17. 5V and 3.3V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU Frequency (3.3V Nominal)	0.75	–	12.6	MHz	12 MHz only for SLIMO Mode = 0
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{IMO12}	Internal Main Oscillator Stability for 12 MHz (Commercial Temperature)[7]	11.4	12	12.6	MHz	Trimmed for 3.3V operation using factory trim values. See Figure 7 on page 14, SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Stability for 6 MHz (Commercial Temperature)	5.70	6.0	6.30	MHz	Trimmed for 3.3V operation using factory trim values. See Figure 7 on page 14, SLIMO Mode = 1.
DC_{IMO}	Duty Cycle of IMO	40	50	60	%	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	

Table 18. 2.7V AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU Frequency (2.7V Nominal)	0.75	–	3.25	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	8	32	96	kHz	
F_{IMO12}	Internal Main Oscillator Stability for 12 MHz (Commercial Temperature)[7]	11.0	12	12.9	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 7 on page 14, SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Stability for 6 MHz (Commercial Temperature)	5.60	6.0	6.40	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 7 on page 14, SLIMO Mode = 1.
DC_{IMO}	Duty Cycle of IMO	40	50	60	%	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	

Note
7. 0 to 70 °C ambient, Vdd = 3.3 V.

Table 19. 2.7V AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU Frequency (2.7V Minimum)	0.75	–	6.3	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	8	32	96	kHz	
F_{IMO12}	Internal Main Oscillator Stability for 12 MHz (Commercial Temperature)[7]	11.0	12	12.9	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 7 on page 14, SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Stability for 6 MHz (Commercial Temperature)	5.60	6.0	6.40	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 7 on page 14, SLIMO Mode = 1.
DC_{IMO}	Duty Cycle of IMO	40	50	60	%	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	

AC General Purpose IO Specifications

Table 20 and Table 21 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

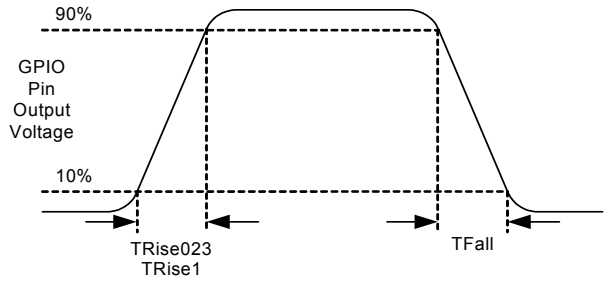
Table 20. 5V and 3.3V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	6	MHz	Normal Strong Mode, Port 1.
TRise023	Rise Time, Strong Mode, Cload = 50 pF Ports 0, 2, 3	15	–	80	ns	Vdd = 3.0 to 3.6V and 4.75V to 5.25V, 10% - 90%
TRise1	Rise Time, Strong Mode, Cload = 50 pF Port 1	10	–	50	ns	Vdd = 3.0 to 3.6V, 10% - 90%
TFall	Fall Time, Strong Mode, Cload = 50 pF All Ports	10	–	50	ns	Vdd = 3.0 to 3.6V and 4.75V to 5.25V, 10% - 90%

Table 21. 2.7V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	1.5	MHz	Normal Strong Mode, Port 1.
TRise023	Rise Time, Strong Mode, Cload = 50 pF Ports 0, 2, 3	15	–	100	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TRise1	Rise Time, Strong Mode, Cload = 50 pF Port 1	10	–	70	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TFall	Fall Time, Strong Mode, Cload = 50 pF All Ports	10	–	70	ns	Vdd = 2.4 to 3.0V, 10% - 90%

Figure 8. GPIO Timing Diagram



AC Comparator Amplifier Specifications

Table 22 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 22. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP}	Comparator Response Time, 50 mV Overdrive			100 200	ns ns	Vdd ≥ 3.0V. 2.4V < Vcc < 3.0V.

AC Analog Mux Bus Specifications

Table 23 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 23. AC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{SW}	Switch Rate	–	–	3.17	MHz	

AC Low Power Comparator Specifications

Table 24 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 24. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

AC External Clock Specifications

Table 25, Table 26, Table 27, and Table 28 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 25. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.750	–	12.6	MHz	
–	High Period	38	–	5300	ns	
–	Low Period	38	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

Table 26. 3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1	0.750	–	12.6	MHz	Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

Table 27. 2.7V (Nominal) AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1	0.750	–	3.08	MHz	Maximum CPU frequency is 3 MHz at 2.7V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater	0.15	–	6.35	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High Period with CPU Clock divide by 1	160	–	5300	ns	
–	Low Period with CPU Clock divide by 1	160	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

Table 28. 2.7V (Minimum) AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1	0.750	–	6.3	MHz	Maximum CPU frequency is 6 MHz at 2.7V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater	0.15	–	12.6	MHz	If the frequency of the external clock is greater than 6 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High Period with CPU Clock divide by 1	160	–	5300	ns	
–	Low Period with CPU Clock divide by 1	160	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

AC Programming Specifications

Table 29 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 29. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	15	–	ms	
T_{WRITE}	Flash Block Write Time	–	30	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	3.6 < Vdd
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ Vdd ≤ 3.6
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	–	–	70	ns	2.4 ≤ Vdd ≤ 3.0

AC SPI Specifications

Table 30 and Table 31 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 30. 5V and 3.3V AC SPI Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{SPIM}	Maximum Input Clock Frequency Selection, Master	–	–	6.3	MHz	Output clock frequency is half of input clock rate.
F_{SPIS}	Maximum Input Clock Frequency Selection, Slave	–	–	2.05	MHz	
T_{SS}	Width of SS_ Negated Between Transmissions	50	–	–	ns	

Table 31. 2.7V AC SPI Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{SPIM}	Maximum Input Clock Frequency Selection, Master	–	–	3.15	MHz	Output clock frequency is half of input clock rate.
F_{SPIS}	Maximum Input Clock Frequency Selection, Slave	–	–	1.025	MHz	
T_{SS}	Width of SS_ Negated Between Transmissions	50	–	–	ns	

AC I^2C Specifications

Table 32 and Table 33 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 32. AC Characteristics of the I^2C SDA and SCL Pins for Vdd ≥ 3.0V

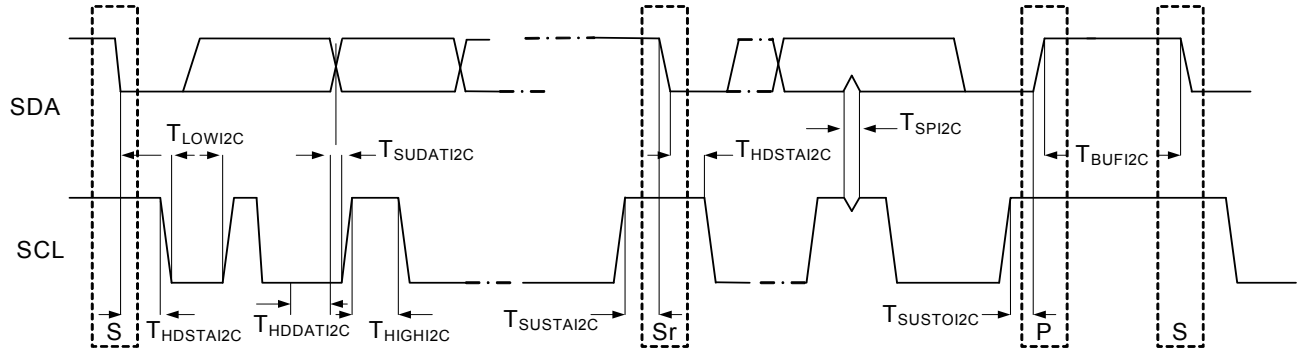
Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
$F_{SCL}I^2C$	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTA}I^2C$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
$T_{LOW}I^2C$	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
$T_{HIGH}I^2C$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
$T_{SUSTA}I^2C$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs
$T_{HDDAT}I^2C$	Data Hold Time	0	–	0	–	µs
$T_{SUDAT}I^2C$	Data Setup Time	250	–	100[8]	–	ns
$T_{SUSTO}I^2C$	Setup Time for STOP Condition	4.0	–	0.6	–	µs
$T_{BUF}I^2C$	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs
$T_{SP}I^2C$	Pulse Width of spikes are suppressed by the input filter	–	–	0	50	ns

Note
8. A Fast Mode I^2C bus device is used in a Standard Mode I^2C bus system but the requirement tSU; DAT Š 250 ns is met. This automatically is the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line trmax + tSU; DAT = 1000 + 250 = 1250 ns (according to the Standard Mode I^2C bus specification) before the SCL line is released.

Table 33. 2.7V AC Characteristics of the I²C SDA and SCL Pins (Fast Mode not Supported)

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
$F_{SCL}I^2C$	SCL Clock Frequency.	0	100	–	–	kHz
$T_{HDSTA}I^2C$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs
$T_{LOW}I^2C$	LOW Period of the SCL Clock.	4.7	–	–	–	µs
$T_{HIGH}I^2C$	HIGH Period of the SCL Clock	4.0	–	–	–	µs
$T_{SUSTA}I^2C$	Setup Time for a Repeated START Condition.	4.7	–	–	–	µs
$T_{HDDAT}I^2C$	Data Hold Time.	0	–	–	–	µs
$T_{SUDAT}I^2C$	Data Setup Time.	250	–	–	–	ns
$T_{SUSTO}I^2C$	Setup Time for STOP Condition.	4.0	–	–	–	µs
$T_{BUF}I^2C$	Bus Free Time Between a STOP and START Condition.	4.7	–	–	–	µs
$T_{SP}I^2C$	Pulse Width of spikes are suppressed by the input filter.	–	–	–	–	ns

Figure 9. Definition for Timing for Fast/Standard Mode on the I2C Bus

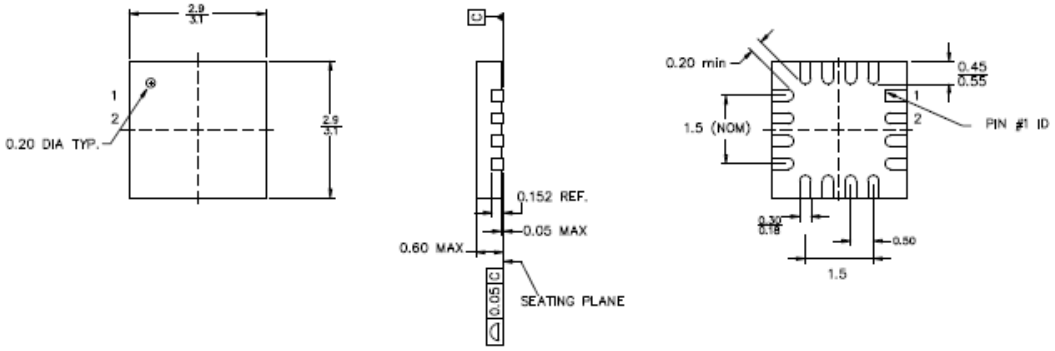


Packaging Dimensions

This section illustrates the packaging specifications for the CY8C20234, CY8C20334, CY8C20434, and CY8C20534 PSoC devices along with the thermal impedances for each package.

It is important to note that emulation tools require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

Figure 10. 16-Pin Chip On Lead 3 X 3 mm Package Outline (Sawn)



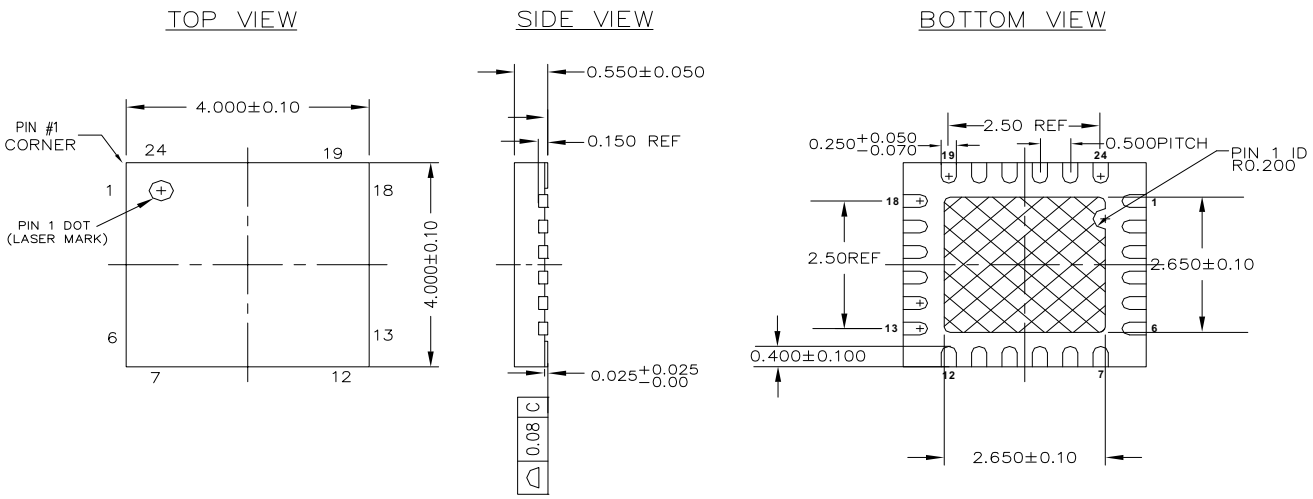
PART NO.	DESCRIPTION
LG16A	LEAD-FREE
LD16A	STANDARD

NOTES:

1. JEDEC # MO-220
2. Package Weight: 0.014g
3. DIMENSIONS IN MM, MIN / MAX

001-09116 *D

Figure 11. 24-Pin (4 x 4 x 0.6 mm) Sawn QFN

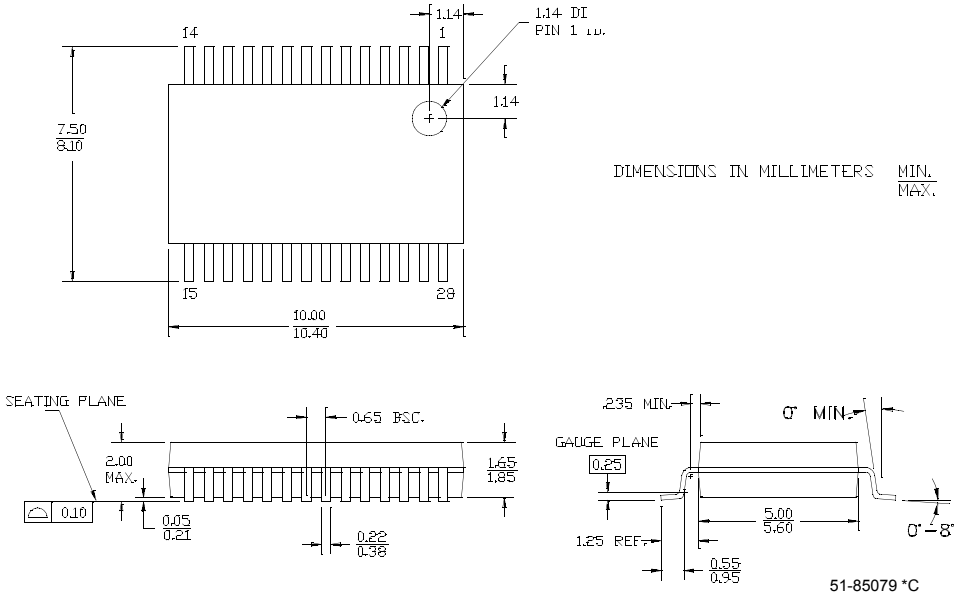


NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. UNIT PACKAGE WEIGHT : 0.024 grams
4. ALL DIMENSIONS ARE IN MILLIMETERS

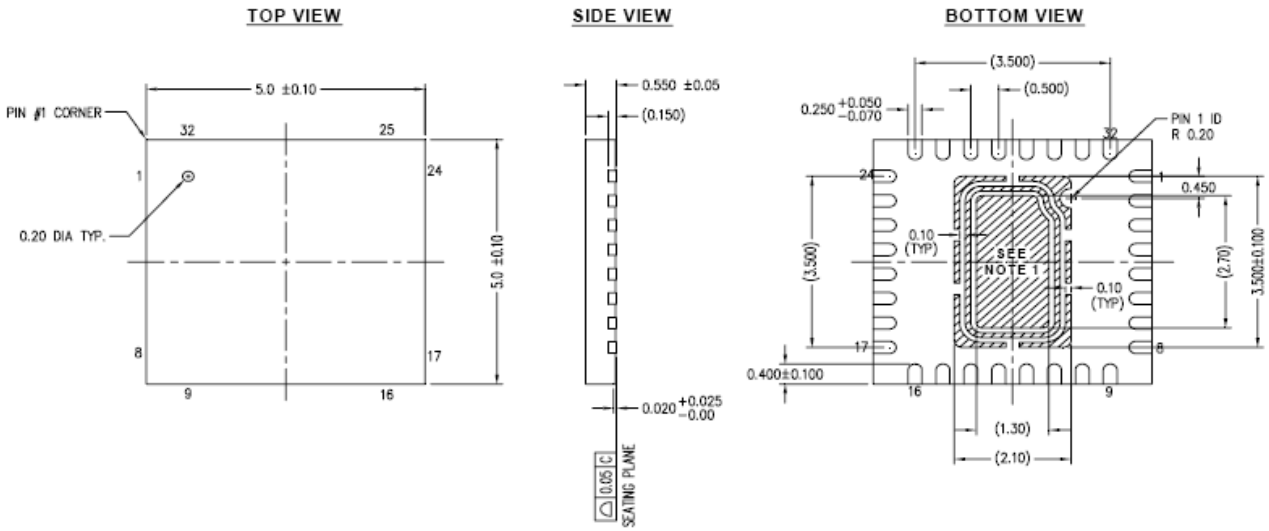
001-13937 *B

Figure 12. 28-Pin (210-Mil) SSOP



51-85079 *C

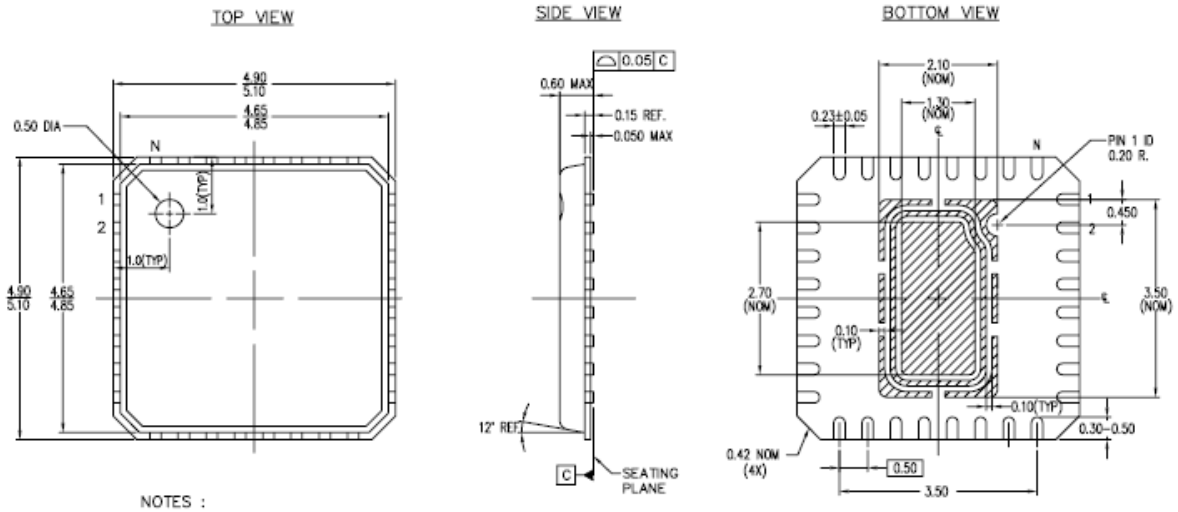
Figure 13. 32-Pin QFN 5 x 5 mmX 0.60 Max (Sawn)



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-48913 *A

Figure 14. 32-Pin (5 x 5 mm 0.60 MAX) QFN



NOTES :

HATCH AREA IS EXPOSED METAL

JEDEC # MO-220

DIMENSIONS IN mm MIN. MAX.

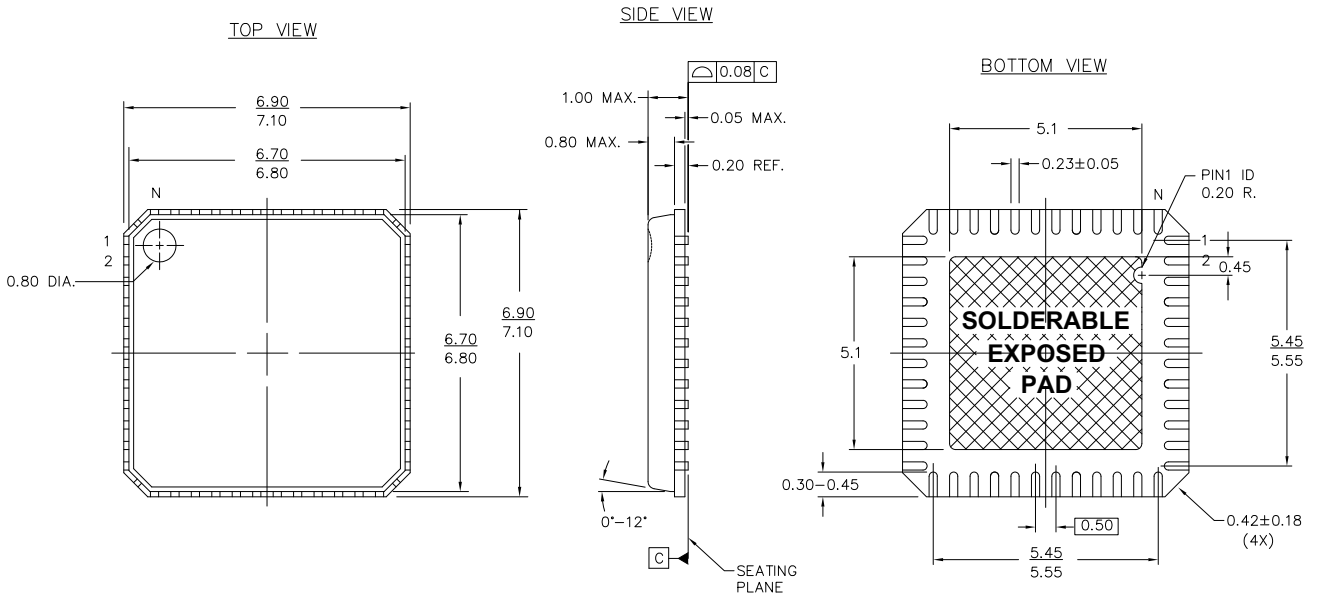
UNIT PACKAGE WEIGHT : 0.0354 Grams

PACKAGE CODE

PART NO.	DESCRIPTION
LJ32B	STANDARD
LK32B	PB-FREE

001-06392 *A

Figure 15. 48-Pin (7 x 7 mm) QFN



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF48A	STANDARD
LY48A	LEAD FREE

001-12919 *A

For information on the preferred dimensions for mounting the QFN packages, see the application note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

It is important to note that pinned vias for thermal conduction are not required for the low power 24, 32, and 48-pin QFN PSoC devices.

Thermal Impedances

Table 34 illustrates the minimum solder reflow peak temperature to achieve good solderability.

Table 34. Thermal Impedances Per Package

Package	Typical θ_{JA} [9]
16 QFN	46 °C/W
24 QFN[10]	25 °C/W
28 SSOP	96 °C/W
32 QFN[10]	27 °C/W
48 QFN[10]	28 °C/W

Solder Reflow Peak Temperature

Table 35 illustrates the minimum solder reflow peak temperature to achieve good solderability.

Table 35. Solder Reflow Peak Temperature

Package	Min Peak Temperature [11]	Max Peak Temperature
16 QFN	240°C	260°C
24 QFN	240°C	260°C
28 SSOP	240°C	260°C
32 QFN	240°C	260°C
48 QFN	240°C	260°C

Notes

9. $T_J = T_A + \text{Power} \times \theta_{JA}$.
10. To achieve the thermal impedance specified for the QFN package, the center thermal pad is soldered to the PCB ground plane.
11. Higher temperatures is required based on the solder melting point. Typical temperatures for solder are 220 ± 5oC with Sn-Pb or 245 ± 5oC with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer. This is used by thousands of PSoC developers. This robust software is facilitating PSoC designs for half a decade. PSoC Designer is available free of charge at http://www.cypress.com under DESIGN RESOURCES >> Software and Drivers.

PSoC Programmer

PSoC Programmer is flexible enough and is used on the bench in development and also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

C Compilers

PSoC Designer comes with a free HI-TECH C Lite C compiler. The HI-TECH C Lite compiler is free, supports all PSoC devices, integrates fully with PSoC Designer and PSoC Express, and runs on Windows versions up to 32-bit Vista. Compilers with additional features are available at additional cost from their manufactures.

- HI-TECH C PRO for the PSoC is available from http://www.htsoft.com.
- ImageCraft Cypress Edition Compiler is available from http://www.imagecraft.com.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

CY3210-ExpressDK PSoC Express Development Kit

The CY3210-ExpressDK is for advanced prototyping and development with PSoC Express (used with ICE-Cube In-Circuit Emulator). It provides access to I^2C buses, voltage reference, switches, upgradeable modules, and more. The kit includes:

- PSoC Express Software CD
- Express Development Board
- Four Fan Modules
- Two Proto Modules
- MiniProg In-System Serial Programmer
- MiniEval PCB Evaluation Board
- Jumper Wire Kit
- USB 2.0 Cable
- Serial Cable (DB9)
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- 2 CY8C24423A-24PXI 28-PDIP Chip Samples
- 2 CY8C27443-24PXI 28-PDIP Chip Samples
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.
Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 36. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit [12]	Foot Kit [13]	Prototyping Module	Adapter [14]
CY8C20234-12LKXI	16 SOIC	-	CY3250-16QFN-FK	CY3210-0X34	-
CY8C20334-12LQXI	24 QFN	CY3250-20334QFN	CY3250-24QFN-FK	CY3210-0X34	AS-24-28-01ML-6
CY8C20534-12PVXI	28 SSOP	-	CY3250-28SSOP-FK	CY3210-0X34	-
CY8C20434-12LKXI	32 QFN	CY3250-20434QFN	CY3250-32QFN-FK	CY3210-0X34	AS-32-28-03ML-6

Third Party Tools

Several tools are specially designed by the following third party vendors to accompany PSoC devices during development and production. Specific details of each of these tools are found at http://www.cypress.com under DESIGN RESOURCES >> Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on emulating the circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see Application Note AN2323 “Debugging - Build a PSoC Emulator into Your Board” at http://www.cypress.com.

Notes
12. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
13. Foot kit includes surface mount feet that is soldered to the target PCB.
14. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters is found at http://www.emulation.com.

Ordering Information

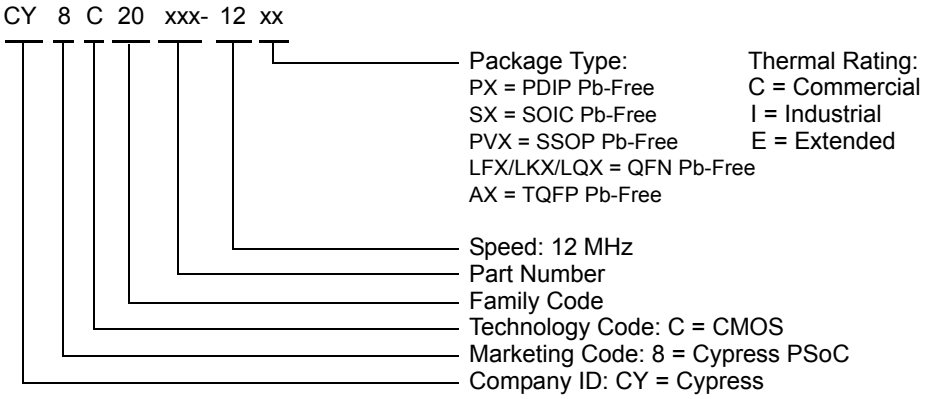
Table 37 lists the CY8C20234, CY8C20334, CY8C20434, and CY8C20534 PSoC device's key package features and ordering codes.

Table 37. PSoC Device Key Features and Ordering Information

Ordering Code	Package	Flash (Bytes)	SRAM (Bytes)	Digital Blocks	CapSense Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
CY8C20234-12LKXI	16-Pin (3x3 mm 0.60 MAX) Sawn QFN	8K	512	0	1	13	13[15]	0	Yes
CY8C20234-12LKXIT	16-Pin (3x3 mm 0.60 MAX) Sawn QFN (Tape and Reel)	8K	512	0	1	13	13[15]	0	Yes
CY8C20334-12LQXI	24-Pin (4x4 mm 0.60 MAX) SAWN QFN	8K	512	0	1	20	20[15]	0	Yes
CY8C20334-12LQXIT	24-Pin (4x4 mm 0.60 MAX) Sawn QFN (Tape and Reel)	8K	512	0	1	20	20[15]	0	Yes
CY8C20434-12LKXI	32-Pin (5x5 mm 0.60 MAX) QFN	8K	512	0	1	28	28[15]	0	Yes
CY8C20434-12LKXIT	32-Pin (5x5 mm 0.60 MAX) QFN (Tape and Reel)	8K	512	0	1	28	28[15]	0	Yes
CY8C20434-12LQXI	32-Pin (5x5 mm 0.60 MAX) Thin Sawn QFN	8K	512	0	1	28	28	0	Yes
CY8C20434-12LQXIT	32-Pin (5x5 mm 0.60 MAX) Thin Sawn QFN (Tape and Reel)	8K	512	0	1	28	28	0	Yes
CY8C20534-PVXI	28-Pin (210-Mil) SSOP	8K	512	0	1	24	24	0	Yes
CY8C20534-PVXIT	28-Pin (210-Mil) SSOP (Tape and Reel)	8K	512	0	1	24	24	0	Yes
CY8C20000-12LFXI	48-Pin OCD QFN[16]	8K	512	0	1	28	28[15]	0	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Figure 16. Ordering Code Definitions



Notes
15. Dual function Digital I/O Pins also connect to the common analog mux.
16. This part may be used for in-circuit debugging. It is NOT available for production.

Document History Page

Document Title: CY8C20234/CY8C20334/CY8C20434/CY8C20534 PSoC® Programmable System-on-Chip™ Document Number: 001-05356				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	404571	HMT	See ECN	New silicon and document (Revision **).
*A	418513	HMT	See ECN	Updated Electrical Specifications, including Storage Temperature and Maximum Input Clock Frequency. Updated Features and Analog System Overview. Modified 32-pin QFN E-PAD dimensions. Added new 32-pin QFN. Add High Output Drive indicator to all P1[x] pinouts. Updated trademarks.
*B	490071	HMT	See ECN	Made data sheet “Final”. Added new Development Tool section. Added OCD pinout and package diagram. Added 16-pin QFN. Updated 24-pin and 32-pin QFN package diagrams to 0.60 MAX thickness. Changed from commercial to industrial temperature range. Updated Storage Temperature specification and notes. Updated thermal resistance data. Added development tool kit part numbers. Finetuned features and electrical specifications.
*C	788177	HMT	See ECN	Added CapSense SNR requirement reference. Added Low Power Comparator (LPC) AC/DC electrical specifications tables. Added 2.7V minimum specifications. Updated figure standards. Updated Technical Training paragraph. Added QFN package clarifications and dimensions. Updated ECN-ed Amkor dimensioned QFN package diagram revisions.
*D	1356805	HMT/SFVTMP3/HCL/SFV	See ECN	Updated 24-pin QFN Theta JA. Added External Reset Pulse Width, TXRST, specification. Fixed 48-pin QFN.vsd. Updated the table introduction and high output voltage description in section two. The sentence: "Exceeding maximum ratings may shorten the battery life of the device.” does not apply to all data sheets. Therefore, the word "battery" is changed to "useful.” Took out tabs after table and figure numbers in titles and added two hard spaces. Updated the section, DC General Purpose IO Specifications on page 16 with new text. Updated VOH5 and VOH6 to say, ”High Output Voltage, Port 1 Pins with 3.0V LDO Regulator Enabled.” Updated VOH7 and VOH8 with the text, “maximum of 20 mA source current in all IOs.”Added 28-pin SSOP part, pinout, package. Updated specs. Modified dev. tool part numbers.

Document History Page (continued)

Document Title: CY8C20234/CY8C20334/CY8C20434/CY8C20534 PSoC® Programmable System-on-Chip™ Document Number: 001-05356				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	2197347	UVS/AESA	See ECN	Added 32-pin Sawn QFN Pin diagram Removed package diagram: 32-Pin (5 X 5 mm) SAWN QFN(001-42168 *A) Updated Ordering Information table with CY8C20434-12LQXI and CY8C20434-12LQXIT ordering details. Corrected Table 16. DC Programming Specifications - Included above the table "Flash Endurance and Retention specifications with the use of the EEPROM User Module are valid only within the range: 25°C +/-20C during the Flash Write operation. Refer the EEPROM User Module data sheet instructions for EEPROM Flash Write requirements outside of the 25°C +/-20°C temperature window."
*F	2542938	RLRM/AESA	07/30/2008	Corrected Ordering Information format. Updated package diagrams 001-13937 and 001-30999. Updated data sheet template. Corrected Figure 6 (28-pin diagram).
*G	2610469	SNV/PYRS	11/20/08	Updated V_{OH5}, V_{OH7}, and V_{OH9} specifications
*H	2693024	DPT/PYRS	04/16/2009	Changed title from PSoC® Mixed Signal Array to PSoC® Programmable System-on-Chip™ Replaced package outline drawing for 32-Pin Sawn QFN Updated "Development Tool Selection" on page 30 Updated "Development Tools" on page 4 and "Designing with PSoC Designer" on page 5 Updated "Getting Started" on page 3

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