4W, 25W Filter-Free Class-D Stereo Amplifier with AM Avoidance

Check for Samples: TPA3131D2, TPA3132D2

FEATURES

- **Supports Multiple Output Configurations**
  - **2×4-W into a 8-Ω BTL Load at 7.4 V (TPA3131D2)**
  - **2×25-W into a 8-Ω BTL Load at 19 V (TPA3132D2)**
- **Wide Voltage Range: 4.5 V – 26 V**
- **Automotive Load-Dump Compliant**
- **Efficient Class-D Operation**
  - **>90% Power Efficiency Combined with Low Idle Loss for Heat Sink free Operation**
  - **Advanced Modulation Schemes**
- **Multiple Switching Frequencies**
  - **AM Avoidance**
  - **Master/Slave Synchronization**
  - **Up to 1.2 MHz Switching Frequency**
- **Feedback Power Stage Architecture with High PSRR Reduces PSU Requirements**
- **Programmable Power Limit**
- **Differential/Single-Ended Inputs**
- **Stereo and Mono Mode with Single Filter Mono Configuration**
- **Single Power Supply Reduces Component Count**
- **Integrated Self-Protection Circuits Including Over-Voltage, Under-Voltage, Over-Temperature, DC-Detect, and Short Circuit with Error Reporting**
- **Thermally Enhanced Package**
  - **32-Pin QFN Pad-Down**
- **–40°C to 85°C Ambient Temperature Range**

APPLICATIONS

- **Laptop Computers and Ultrabooks**
- **Flatpanel TV**
- **Consumer Audio Applications**

DESCRIPTION

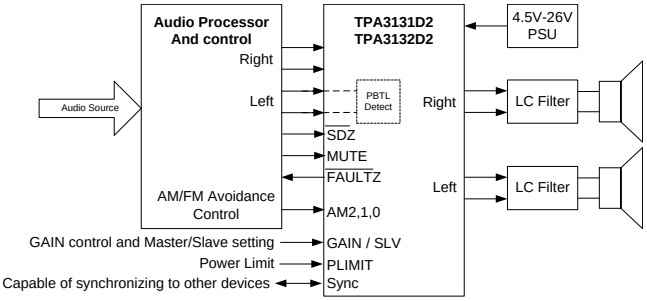
The TPA3131/32D2 are efficient, stereo digital amplifier power stages for driving speakers with up to 2x42W/4Ω peak power. TPA3131/32D2 operates heatsink-free with cooling to PCB through the bottom side Power-Pad with sustained output power from 2x4W/8Ω (TPA3131D2) to 2x25W/8Ω (TPA3132D2).

The TPA3131/32D2 advanced oscillator/PLL circuit employs a multiple switching frequency option to avoid AM interferences; this is achieved together with an option of Master/Slave option, making it possible to synchronize multiple devices.

The TPA3131/32D2 are fully protected against faults with short-circuit protection and thermal protection as well as over-voltage, under-voltage and DC protection. Faults are reported back to the processor to prevent devices from being damaged during overload conditions.

For feature compatible devices see: Power Pad up device 2x50W TPA3116D2, Power Pad down 2x15W TPA3130D2 and 2x30W TPA3118D2.

Simplified Application Circuit

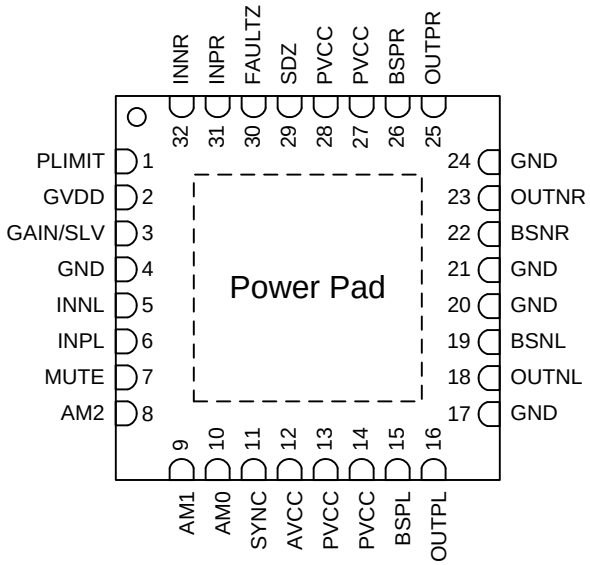


DEVICE	POWER	QFN 32-PIN
TPA3131D2	2 x 4W/8Ω	Pad down
TPA3132D2	2 x 25W/8Ω	Pad down

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CONNECTION DIAGRAM

QFN PACKAGE
32-PIN
(TOP VIEW)



TERMINAL FUNCTIONS

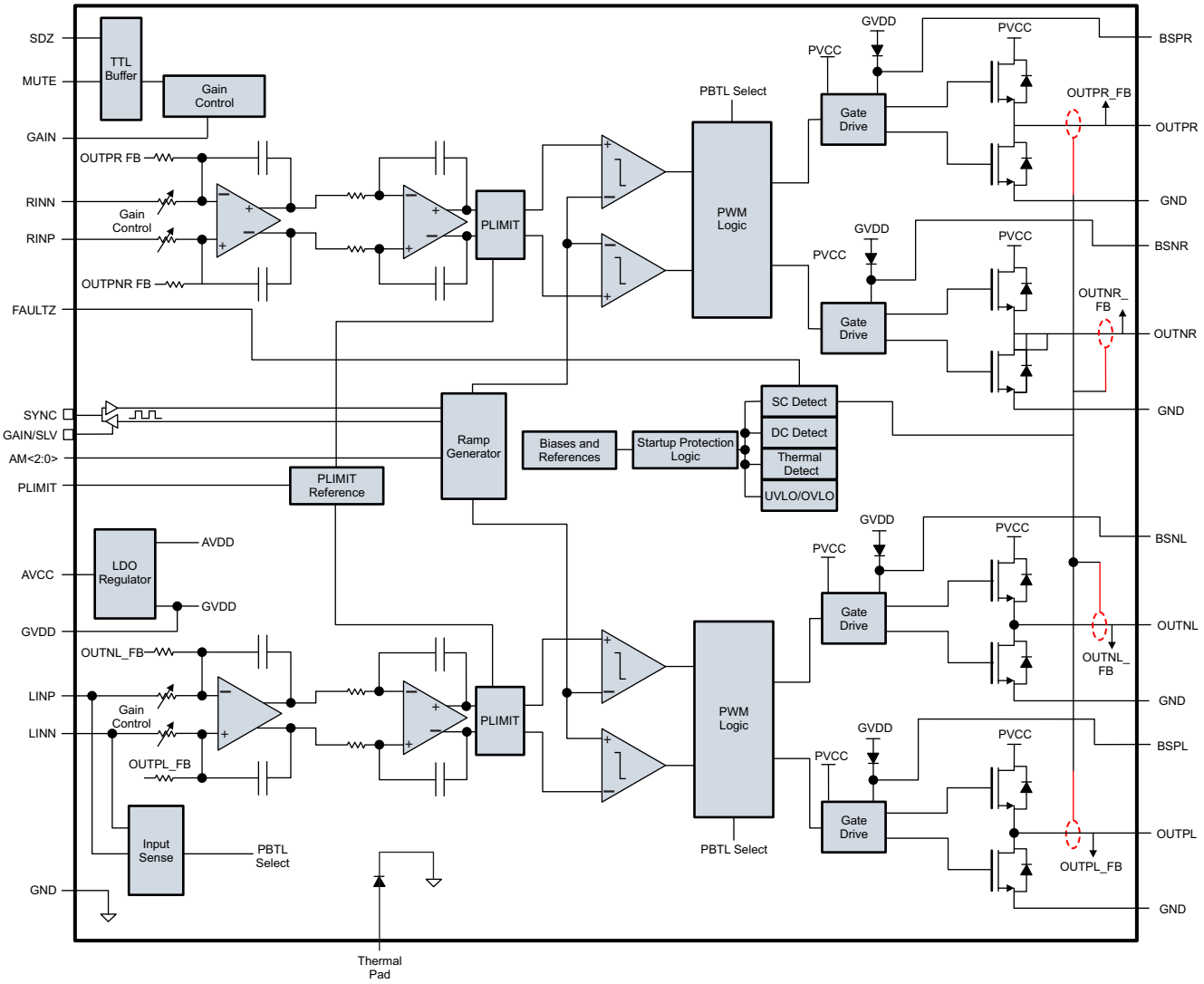
PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	PLIMIT	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
2	GVDD	PO	Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1uF X7R ceramic decoupling capacitor.
3	GAIN/SLV	I	Sets Gain and selects between Master and Slave mode depending on pin voltage divider.
4	GND	G	Ground
5	INNL	I	Negative audio input for left channel. Biased at 3V.
6	INPL	I	Positive audio input for left channel. Biased at 3V.
7	MUTE	I	Mute signal for fast disable/enable of outputs: HIGH = outputs OFF (high-Z), LOW = outputs ON. TTL logic levels with compliance to AVCC.
8	AM2	I	AM Avoidance Frequency Selection
9	AM1	I	AM Avoidance Frequency Selection
10	AM0	I	AM Avoidance Frequency Selection
11	SYNC	DIO	Clock input/output for synchronizing multiple class-D devices. Direction determined by GAIN/SLV pin. Input signal not to exceed GVDD (7V)
12	AVCC	P	Analog Supply
13	PVCC	P	Power supply
14	PVCC	P	Power supply
15	BSPL	BST	Boot strap for positive left channel output, connect to 220nF X7R ceramic cap to OUTPL
16	OUTPL	PO	Positive left channel output
17	GND	G	Ground
18	OUTNL	PO	Negative left channel output

(1) **TYPE**: DO = Digital Output, I = Analog Input, G = General Ground, PO = Power Output, BST = Boot Strap.

TERMINAL FUNCTIONS (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
19	BSNL	BST	Boot strap for negative left channel output, connect to 220nF X7R ceramic cap to OUTNL
20	GND	G	Ground
21	GND	G	Ground
22	BSNR	BST	Boot strap for negative right channel output, connect to 220nF X7R ceramic cap to OUTNR
23	OUTNR	PO	Negative right channel output
24	GND	G	Ground
25	OUTPR	PO	Positive right channel output
26	BSPR	BST	Boot strap for positive right channel output, connect to 220nF X7R ceramic cap to OUTPR
27	PVCC	PI	Power supply
28	PVCC	PI	Power supply
29	SDZ	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
30	FAULTZ	DO	General fault reporting including Over-current_PVCC, OVP_DVDD FAULT1Z = High, normal operation FAULT1Z = Low, fault condition
31	INPR	I	Positive audio input for right channel. Biased at 3V.
32	INNR	I	Negative audio input for right channel. Biased at 3V.
33	Thermal Pad or PowerPAD™	G	Connect to GND for best system performance. If not connected to GND, leave floating.

SYSTEM BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage, V_{CC}	PV_{CC}, AV_{CC}	–0.3 to 30	V
Input voltage, V_I	INPL, INNL, INPR, INNR	–0.3 to 6.3	V
	PLIMIT, GAIN / SLV, SYNC	–0.3 to GVDD+0.3	V
	AM0, AM1, AM2, MUTE, SDZ	–0.3 to PVCC+0.3	V
Slew rate, maximum	AM0, AM1, AM2, MUTE, SDZ	10	V/msec
Operating free-air temperature, T_A		–40 to 85	°C
Operating junction temperature range, T_J		–40 to 150	°C
Storage temperature range, T_{stg}		–40 to 125	°C
Electrostatic discharge: Human body model, ESD		±2	kV
Electrostatic discharge: Charged device model, ESD		±500	V

THERMAL INFORMATION

THERMAL METRIC(1)		TPA3131D2 TPA3132D2 QFN 32 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	31.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter(3)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(4)	5.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	PV_{CC}, AV_{CC}	4.5		26	V
V_{IH}	High-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC	2			V
V_{IL}	Low-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC			0.8	V
V_{OL}	Low-level output voltage	FAULTZ, $R_{PULL-UP}$ = 100 kΩ, PV_{CC} = 26 V			0.8	V
I_{IH}	High-level input current	AM0, AM1, AM2, MUTE, SDZ (V_I = 2 V, V_{CC} = 18 V)			50	µA
R_L(BTL)	Minimum load Impedance	Output filter: L = 10 µH, C = 680 nF	3.2	4		Ω
R_L(PBTL)		Output filter: L = 10 µH, C = 1 µF	1.6			
L_o	Output-filter Inductance	Minimum output filter inductance under short-circuit condition	1			µH

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, AV_{CC} = PV_{CC} = 7.4 V to 26 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
| V_{OS} |	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB		1.5	15	mV
I_{CC}	Quiescent supply current	SDZ = 2 V, No load or filter, PV_{CC} = 7.4 V (TPA3131D2)		16		mA
		SDZ = 2 V, No load or filter, PV_{CC} = 19 V (TPA3132D2)		27		
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SDZ = 0.8 V, No load or filter		<50		µA
$r_{DS(on)}$	Drain-source on-state resistance, measured pin to pin	PV_{CC} = 7.4V to 19V V, I_{out} = 500 mA, T_J = 25°C		120		mΩ
G	Gain (BTL)	R1 = open, R2 = 20 kΩ	19	20	21	dB
		R1 = 100 kΩ, R2 = 20 kΩ	25	26	27	
		R1 = 100 kΩ, R2 = 39 kΩ	31	32	33	dB
		R1 = 75 kΩ, R2 = 47 kΩ	35	36	37	
G	Gain (SLV)	R1 = 51 kΩ, R2 = 51 kΩ	19	20	21	dB
		R1 = 47 kΩ, R2 = 75 kΩ	25	26	27	
		R1 = 39 kΩ, R2 = 100 kΩ	31	32	33	dB
		R1 = 16 kΩ, R2 = 100 kΩ	35	36	37	
t_{on}	Turn-on time	SDZ = 2 V		10		ms
t_{OFF}	Turn-off time	SDZ = 0.8 V		2		µs
GVDD	Gate drive supply	IGVDD < 200 µA	6.4	6.9	7.4	V
V_O	Output voltage maximum under PLIMIT control	V(PLIMIT) = 2 V; V_I = 1 V_{rms}	6.75	7.90	8.75	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, AV_{CC} = PV_{CC} = 7.4 V to 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
KSVR	Power supply ripple rejection	200 mV_{PP} ripple at 1 kHz, Gain = 20 dB, Inputs AC-coupled to GND		–70		dB
P_O	Continuous output power	R_L = 8 Ω, THD+N = 10%, f = 1 kHz, PV_{CC} = 7.4 V (TPA3131D2)		4		W
		R_L = 4 Ω, THD+N = 10%, f = 1 kHz, PV_{CC} = 7.4 V (TPA3131D2)		7.3		
		R_L = 8 Ω, THD+N = 10%, f = 1 kHz, PV_{CC} = 19V (TPA3132D2)		25		
		R_L = 4 Ω, THD+N = 10%, f = 1 kHz, PV_{CC} = 19V (TPA3132D2)		42		
THD+N	Total harmonic distortion + noise	R_L = 8 Ω, f = 1 kHz, P_O = 0.1W to 2 W (TPA3132D2) R_L = 8 Ω, f = 1 kHz, P_O = 0.1W to 12.5 W (TPA3131D2)		0.1%		
Vn	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		70		µV
				–80		dBV
	Crosstalk	V_O = 1 V_{rms}, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted (TPA3131D2, PV_{CC} = 7.4V)		98		dB
		Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted (TPA3131D2, PV_{CC} = 19V)		105		

AC ELECTRICAL CHARACTERISTICS (continued)

T_A = 25°C, AV_{CC} = PV_{CC} = 7.4 V to 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	AM2=0, AM1=0, AM0=0	376	400	424	kHz
		AM2=0, AM1=0, AM0=1	470	500	530	
		AM2=0, AM1=1, AM0=0	564	600	636	
		AM2=0, AM1=1, AM0=1	940	1000	1060	
		AM2=1, AM1=0, AM0=0	1128	1200	1278	
		AM2=1, AM1=0, AM0=1	Reserved			
		AM2=1, AM1=1, AM0=0				
		AM2=1, AM1=1, AM0=1				
	Thermal trip point			150+		°C
	Thermal hysteresis			15		°C
	Over current trip point	TPA3131D2		3.4		A
		TPA3132D2		7		

TYPICAL CHARACTERISTICS

f_s = 400 kHz, BD Mode (unless otherwise noted)

TOTAL HARMONIC DISTORTION +NOISE (BTL) vs OUTPUT POWER

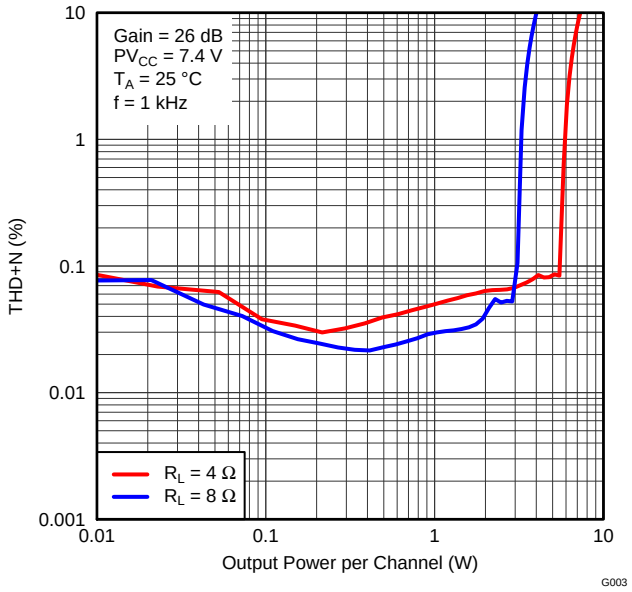


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY

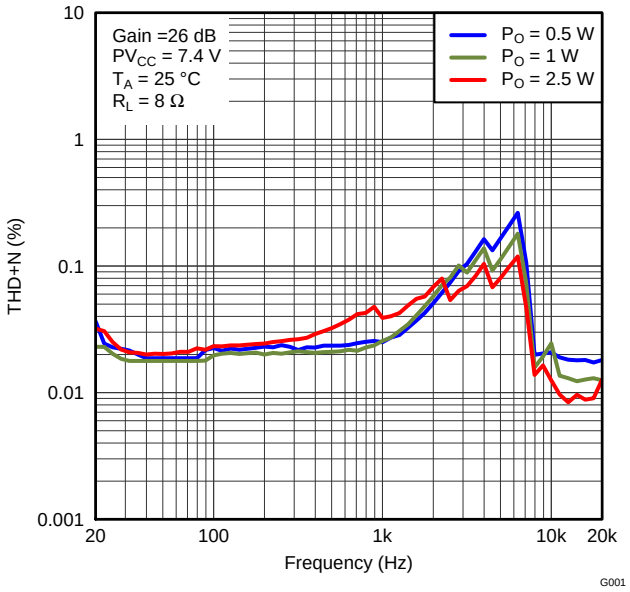


Figure 2.

POWER EFFICIENCY (BTL) vs SUPPLY VOLTAGE

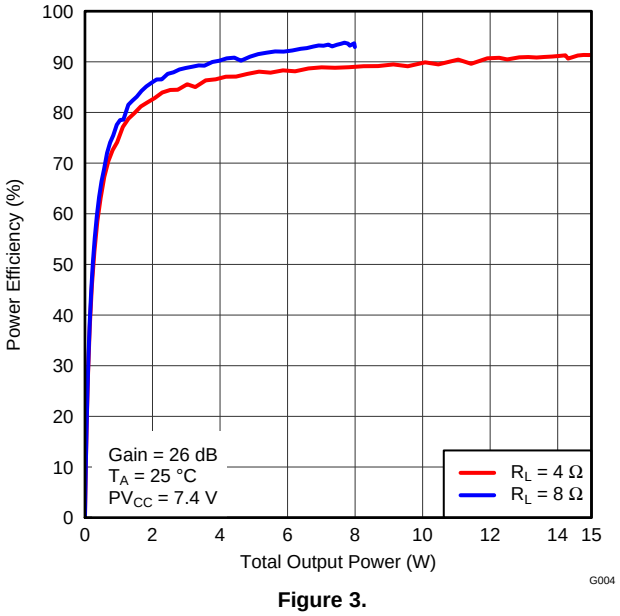


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY

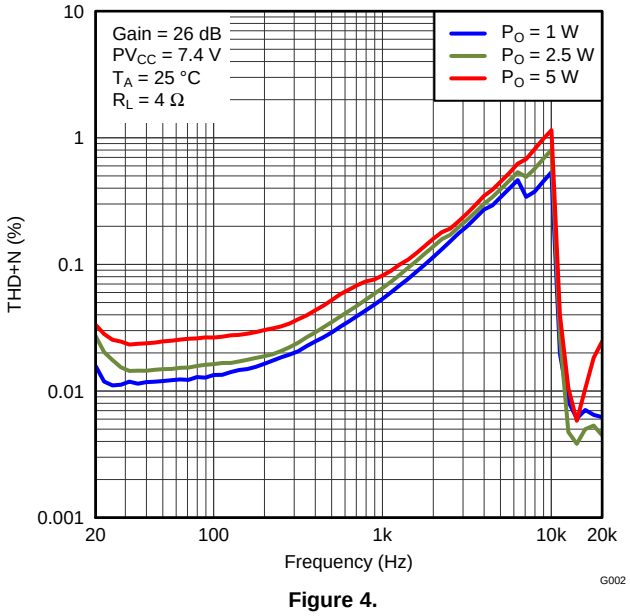


Figure 4.

TYPICAL CHARACTERISTICS (continued)

f_s = 400 kHz, BD Mode (unless otherwise noted)

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER

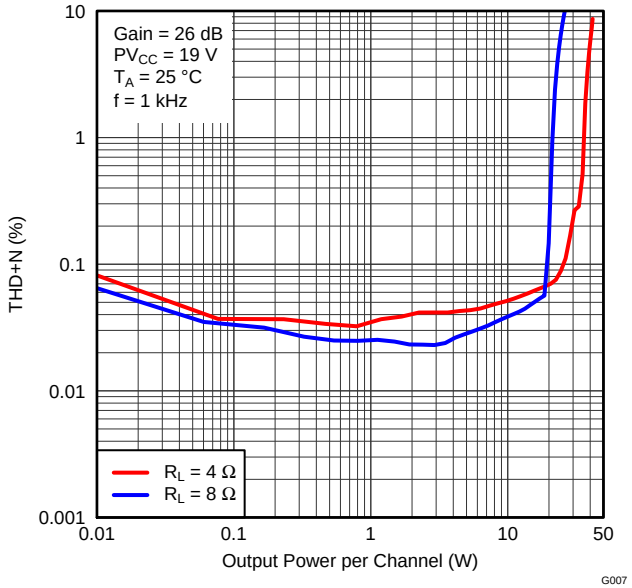


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY

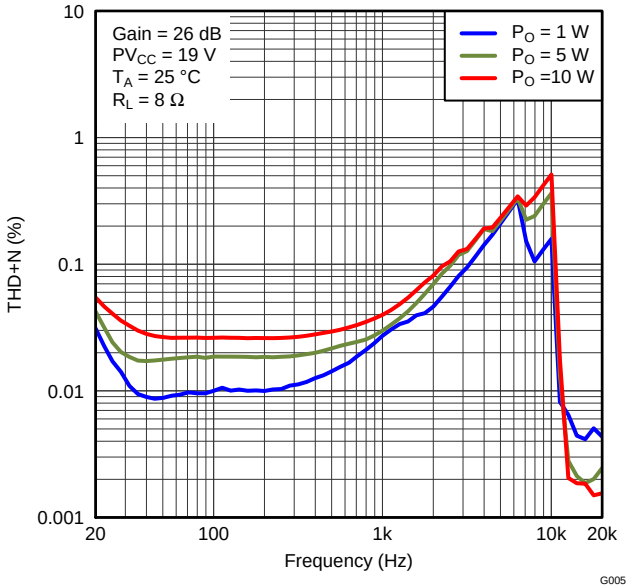


Figure 6.

POWER EFFICIENCY (BTL) vs OUTPUT POWER

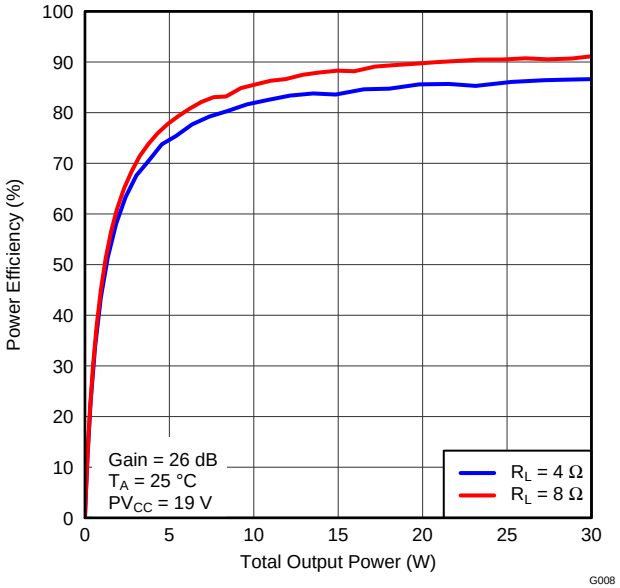


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY

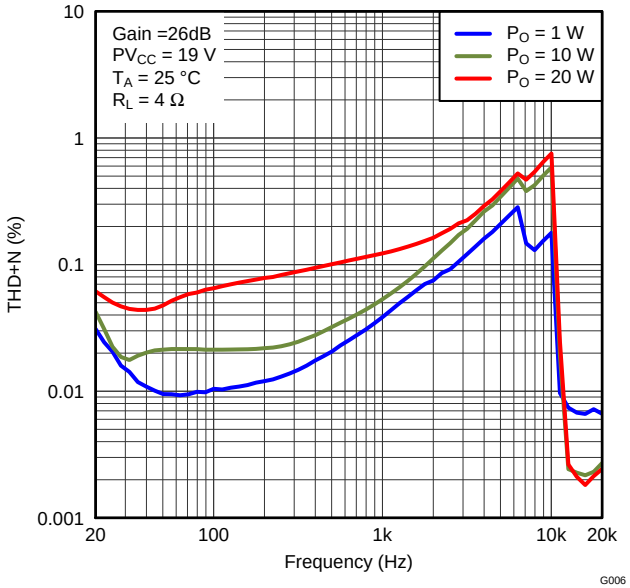


Figure 8.

TYPICAL CHARACTERISTICS (continued)

f_s = 400 kHz, BD Mode (unless otherwise noted)

TOTAL HARMONIC DISTORTION + NOISE (TPA3132D2 PBTL) vs OUTPUT POWER

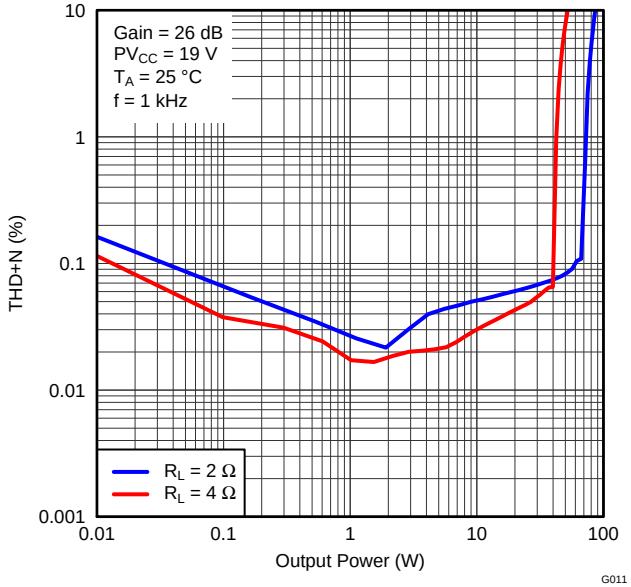


Figure 9.

TOTAL HARMONIC DISTORTION + NOISE (TPA3132D2 PBTL) vs FREQUENCY

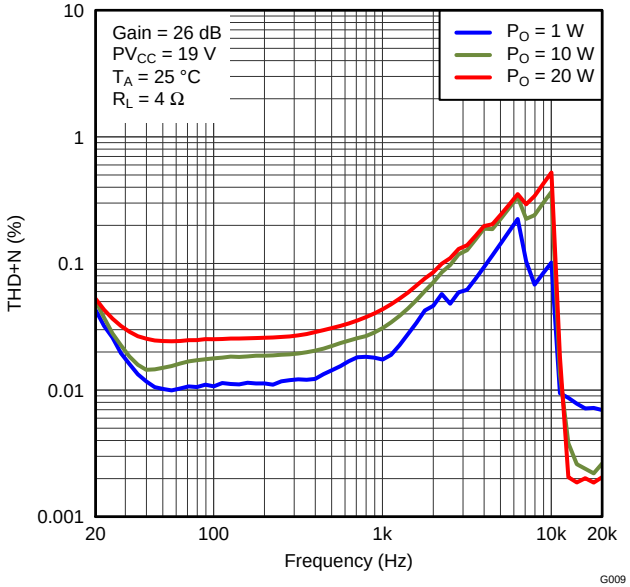


Figure 10.

POWER EFFICIENCY (TPA3132D2 PBTL) vs OUTPUT POWER

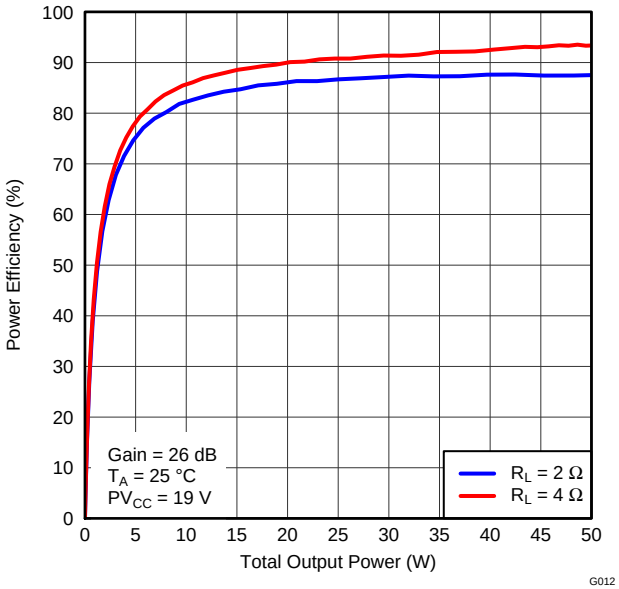


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE (TPA3132D2 PBTL) vs FREQUENCY

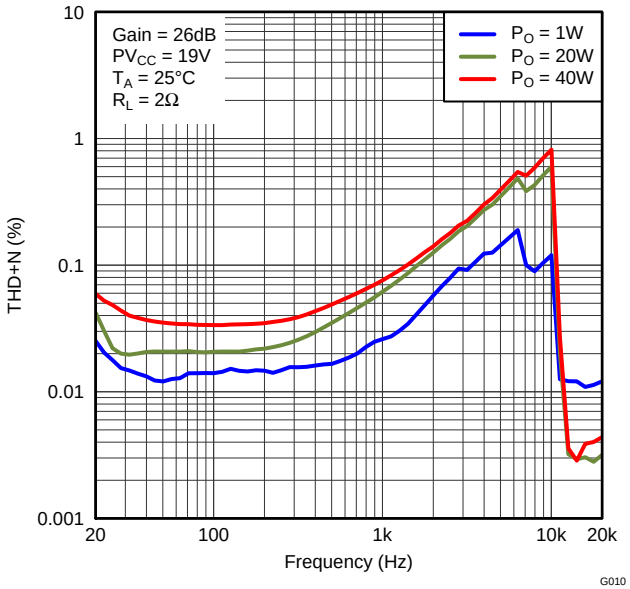


Figure 12.

TYPICAL CHARACTERISTICS (continued)

f_s = 400 kHz, BD Mode (unless otherwise noted)

MAXIMUM OUTPUT POWER (BTL) vs PLIMIT VOLTAGE

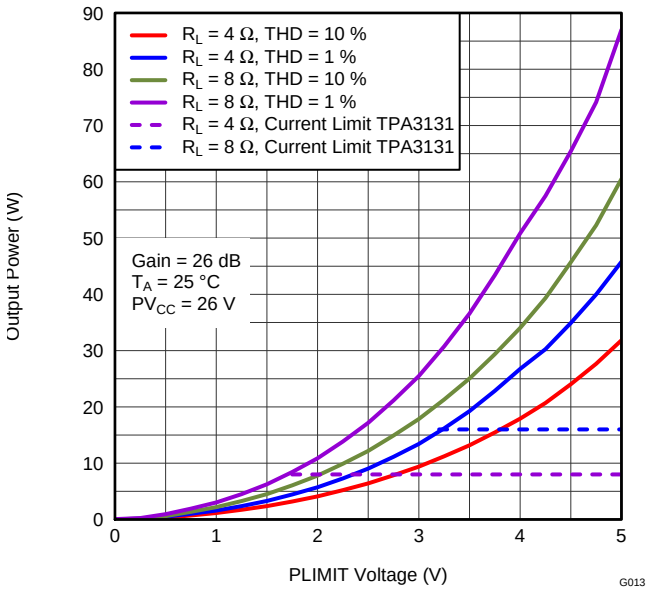


Figure 13.

GAIN/PHASE (BTL) vs FREQUENCY

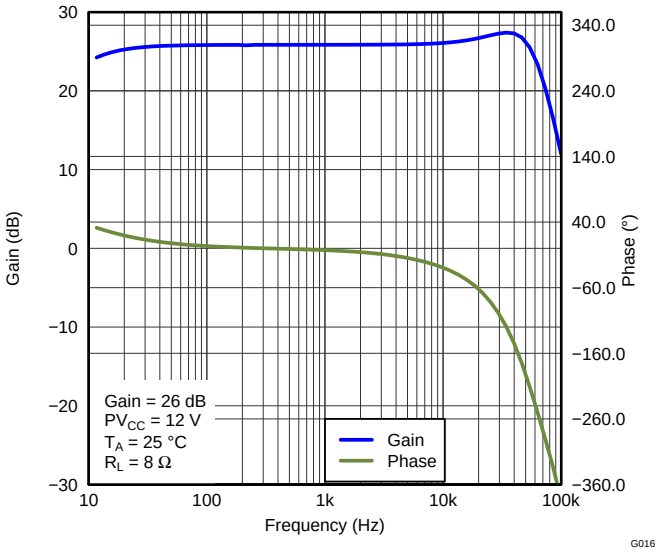


Figure 14.

MAXIMUM OUTPUT POWER (BTL) vs SUPPLY VOLTAGE

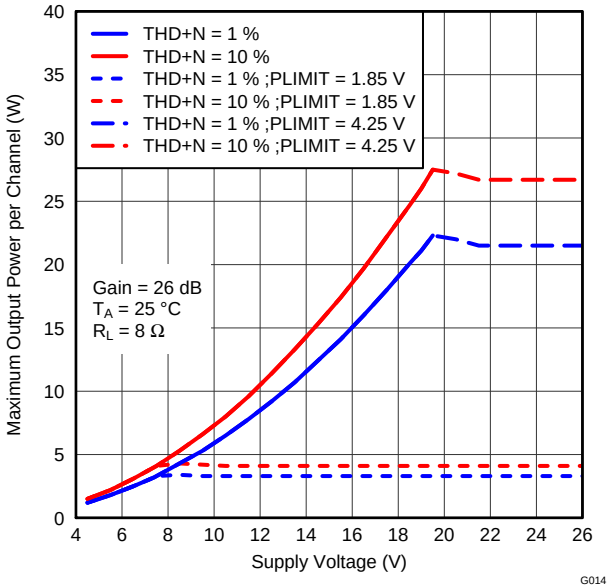


Figure 15.

MAXIMUM OUTPUT POWER (BTL) vs SUPPLY VOLTAGE

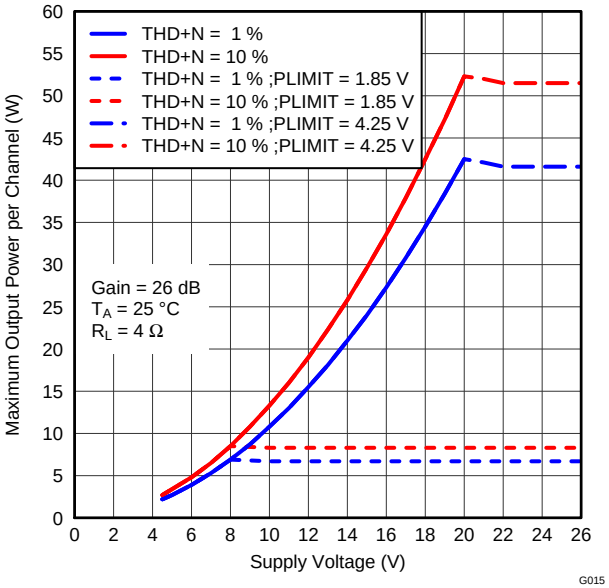


Figure 16.

TYPICAL CHARACTERISTICS (continued)

f_s = 400 kHz, BD Mode (unless otherwise noted)

CROSSTALK (BTL) vs FREQUENCY

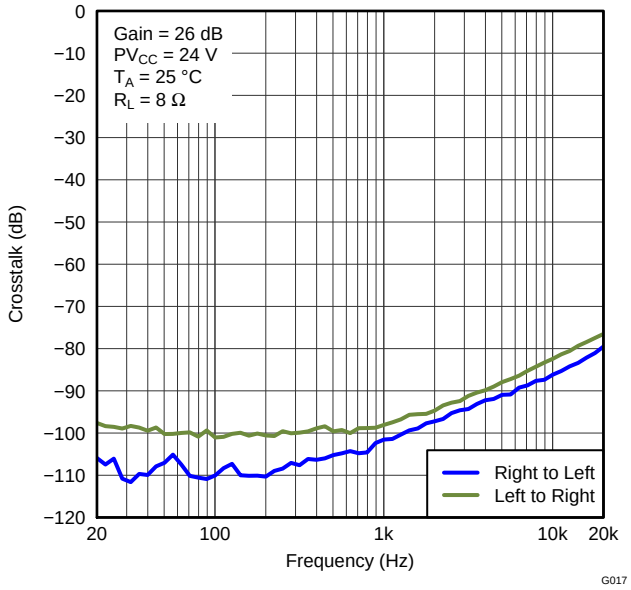


Figure 17.

PSRR vs FREQUENCY

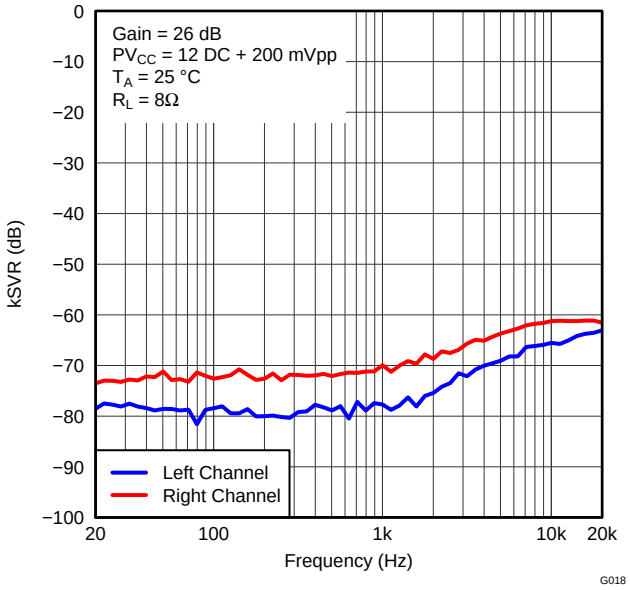
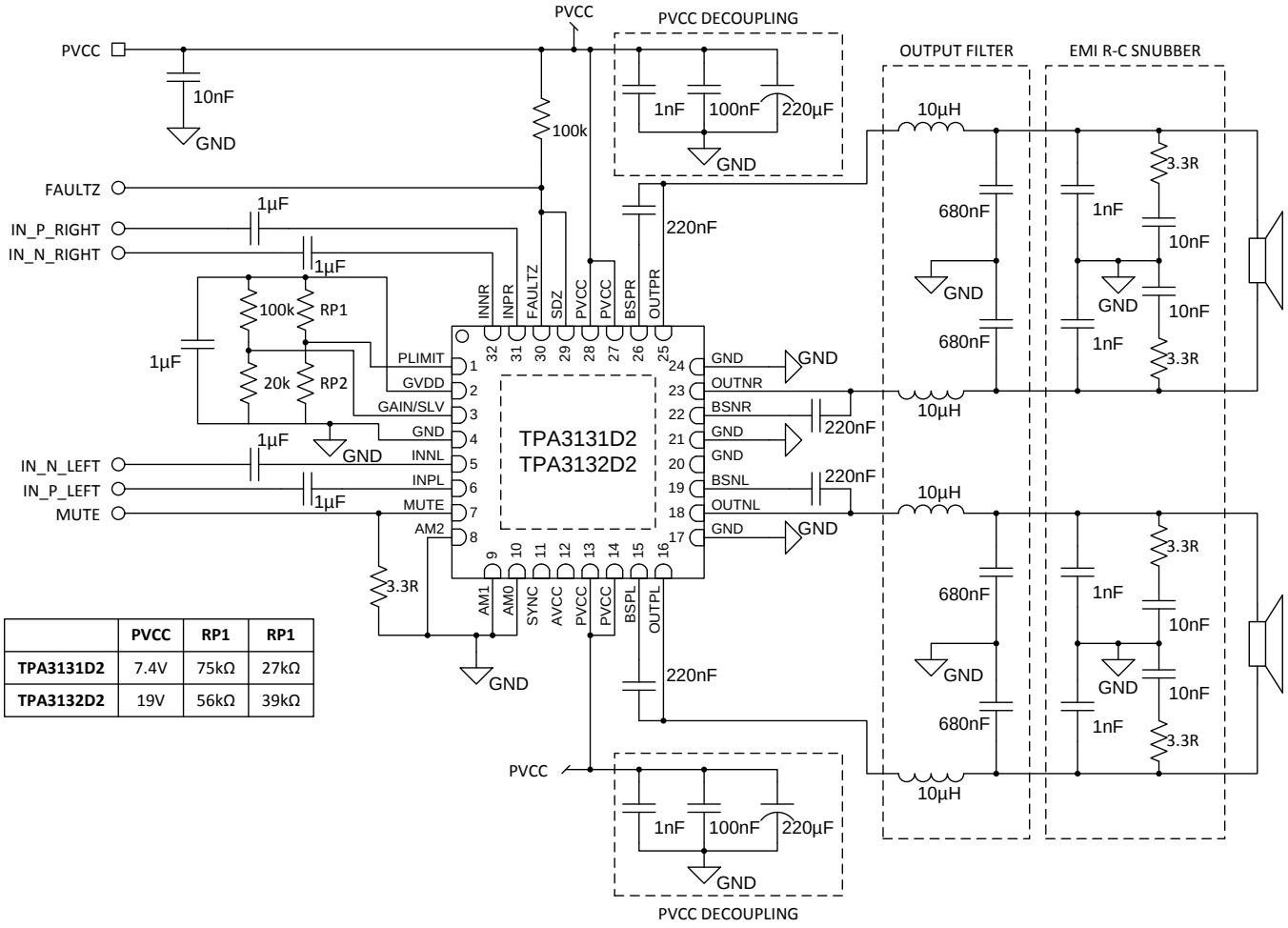


Figure 18.

DEVICE INFORMATION

TYPICAL APPLICATION



	PVCC	RP1	RP1
TPA3131D2	7.4V	75kΩ	27kΩ
TPA3132D2	19V	56kΩ	39kΩ

Figure 19. Typical Application Schematic

GAIN SETTING AND MASTER / SLAVE

The gain of the TPA3131D2 is set by the voltage divider connected to the GAIN/SLV control pin. Master or Slave mode is also controlled by the same pin. An internal ADC is used to detect the 8 input states. The first four stages sets the GAIN in Master mode in gains of 20, 26, 32, 36 dB respectively, while the next four stages sets the GAIN in Slave mode in gains of 20, 26, 32, 36 dB respectively. The gain setting is latched during power-up and cannot be changed while device is powered. shows the recommended resistor values and the state and gain:

Table 1. GAIN and MASTER/SLAVE

MASTER / SLAVE MODE	GAIN	R1 (to GND)	R2 (to GVDD)	INPUT IMPEDANCE
Master	20 dB	5.6 kΩ	OPEN	60 kΩ
Master	26 dB	20 kΩ	100 kΩ	30 kΩ
Master	32 dB	39 kΩ	100 kΩ	15 kΩ
Master	36 dB	47 kΩ	75 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	26 dB	75 kΩ	47 kΩ	30 kΩ

Table 1. GAIN and MASTER/SLAVE (continued)

MASTER / SLAVE MODE	GAIN	R1 (to GND)	R2 (to GVDD)	INPUT IMPEDANCE
Slave	32 dB	100 kΩ	39 kΩ	15 kΩ
Slave	36 dB	100 kΩ	16 kΩ	9 kΩ

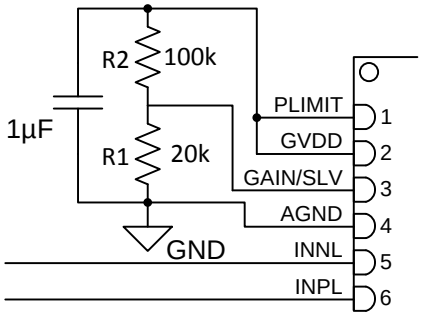


Figure 20. Gain and Master/Slave Select Resistors

In Master mode, SYNC terminal is an output, in Slave mode, SYNC terminal is an input for a clock input. TTL logic levels with compliance to GVDD.

INPUT IMPEDANCE

The TPA3131/32D2 input stage is a fully differential input stage and the input impedance changes with the gain setting from 9 kΩ at 36 dB gain to 60 kΩ at 20 dB gain. Table 1 lists the values from min to max gain. The tolerance of the input resistor value is ±20% so the minimum value will be higher than 7.2 kΩ. The inputs need to be AC-coupled to minimize the output dc-offset and ensure correct ramping of the output voltages during power-ON and power-OFF. The input ac-coupling capacitor together with the input impedance forms a high-pass filter with the following cut-off frequency:

$$f = \frac{1}{2\pi Z_i C_i} \quad (1)$$

If a flat bass response is required down to 20 Hz the recommended cut-off frequency is a tenth of that, 2 Hz. lists the recommended ac-couplings capacitors for each gain step. If a -3 dB is accepted at 20 Hz 10 times lower capacitors can used – for example, a 1 µF can be used.

Table 2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	60 kΩ	1.5 µF	1.8 Hz
26 dB	30 kΩ	3.3 µF	1.6 Hz
32 dB	15 kΩ	5.6 µF	2.3 Hz
36 dB	9 kΩ	10 µF	1.8 Hz

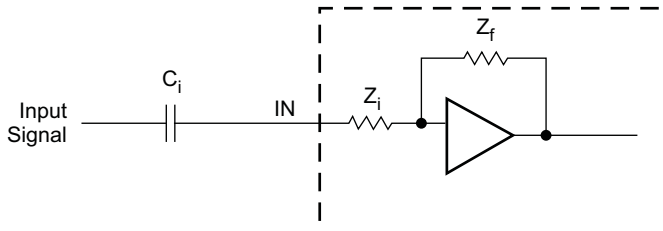


Figure 21. Input AC Coupling

The input capacitors used should be a type with low leakage, like quality electrolytic, tantalum or ceramic. If a polarized type is used the positive connection should face the input pins which are biased to 3 Vdc.

START-UP/SHUTDOWN OPERATION

The TPA3131/32D2 employs a shutdown mode of operation designed to reduce supply current (Icc) to the absolute minimum level during periods of nonuse for power conservation. The SDZ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling SDZ low will put the outputs to mute and the amplifier to enter a low-current state. It is not recommended to leave SDZ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply. The gain setting is selected at the end of the start-up cycle. At the end of the start-up cycle, the gain is selected and cannot be changed until the next power-up.

PLIMIT OPERATION

The TPA3131/32D2 has a built-in voltage limiter that can be used to limit the output voltage level below the supply rail, the amplifier simply operates as if it was powered by a lower supply voltage, and thereby limits the output power. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Add a 1 µF capacitor from pin PLIMIT to ground to ensure stability.

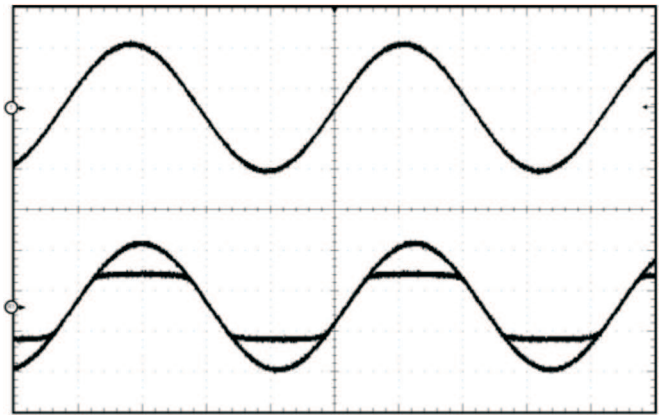


Figure 22. POWER LIMIT Example

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to a fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. This "virtual" rail is approximately 4 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power} \tag{2}$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
R_L is the load resistance.
V_P is the peak amplitude
$V_P = 4 \times$ PLIMIT voltage if PLIMIT $< 4 \times V_P$
P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)

Increasing the PLIMIT voltage from a given value increases the maximum output voltage swing until it equals PVCC. Adjusting PLIMIT to a higher value will disable the PLIMIT function and will offer highest available output power, however for TPA3131D2 and TPA3132D2 it is always advised to use the PLIMIT function if PVCC is higher than nominal value to prevent shutdown due to over current protection. If PLIMIT is disabled on TPA3131D2 and TPA3132D2 an over current shutdown can occur with minimum recommended load impedance when PVCC is higher than its nominal value. To disable the PLIMIT function, the PLIMIT pin is simply connected to GVDD.

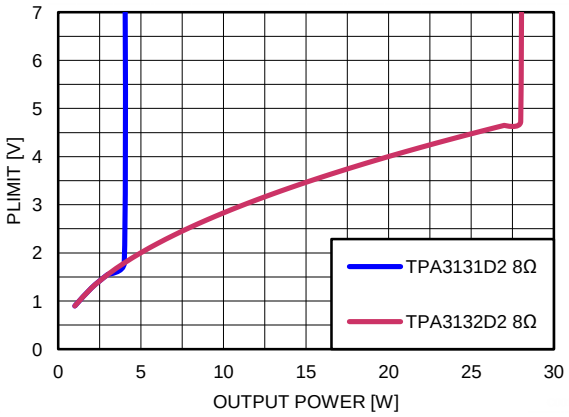


Figure 23. PLIMIT vs. Max. Output Power, 8Ω load

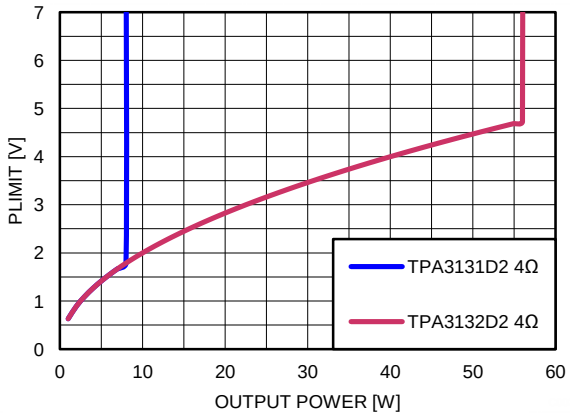


Figure 24. PLIMIT vs. Max. Output Power, 4Ω load

Table 3. POWER LIMIT Example

MINIMUM PV_{CC} (V)	PART NUMBERS	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	OUTPUT POWER 8Ω (W)
7.4 V	TPA3131D2, TPA3132D2	1.85	27 kΩ	75 kΩ	4
12 V	TPA3132D2	2.87	39 kΩ	56 kΩ	10
19 V	TPA3132D2	4.26	56 kΩ	36 kΩ	25

(1) PLIMIT measurements taken with EVM gain set to 26dB and input level adjusted for 10% THD.

GVDD SUPPLY

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also be used to supply the PLIMIT and GAIN/SLV voltage dividers. Decouple GVDD with a X5R ceramic 1 µF capacitor to GND. The GVDD supply is not intended to be used for external supply. It is recommended to limit the current consumption by using resistor voltage dividers for GAIN/SLV and PLIMIT of 100 kΩ or more.

BSPx AND BSNx CAPACITORS

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220 nF ceramic capacitor of quality X5R or better, rated for at least 16 V, must be connected from each output to its corresponding bootstrap input. (See the application circuit diagram in Figure 19.) The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

DIFFERENTIAL INPUTS

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3131/32D2 with a differential source, connect the positive lead of the audio source to the RINP or LINP input and the negative lead from the audio source to the RINN or LINN input. To use the TPA3131/32D2 with a single-ended source, ac ground the negative input through a capacitor equal in value to the input capacitor on positive and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the 10 ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

MONO MODE (PBTL)

The TPA3131/32D2 can be connected in MONO mode enabling up to 85W output power. This is done by:

- Connect INPL and INNL directly to Ground (without capacitors) this sets the device in Mono mode during power up.
- Connect OUTPR and OUTNR together for the positive speaker terminal and OUTNL and OUTPL together for the negative terminal.
- Analog input signal is applied to INPR and INNR.

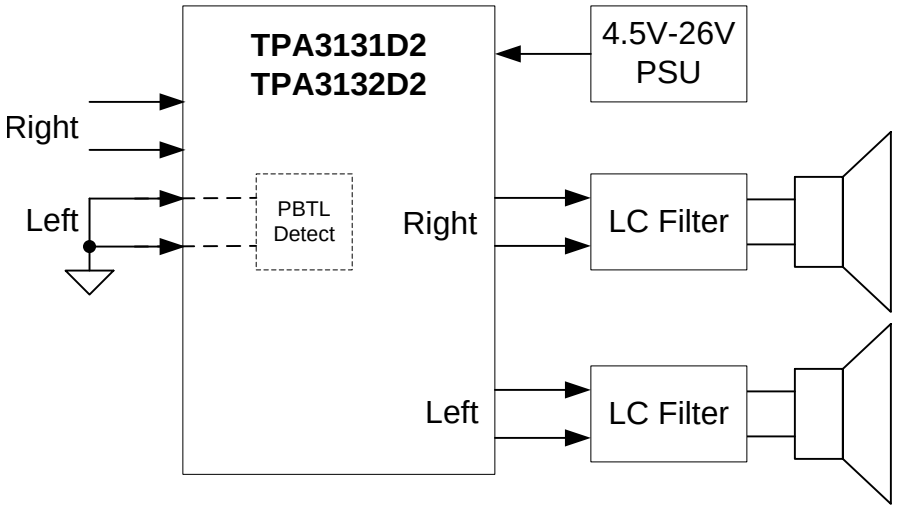


Figure 25. OUTPUT MODE SELECT

DEVICE PROTECTION SYSTEM

The TPA3131/32D2 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, over temperature, and under-voltage. The FAULTZ pin will signal if an error is detected according to the fault table below:

Table 4. Fault Reporting

FAULT	TRIGGERING CONDITION (typical value)	FAULTZ	ACTION	LATCHED/SELF-CLEARING
Over Current	Output short or short to PVCC or GND	Low	Output high impedance	Latched
Over Temperature	T_j > 150°C	Low	Output high impedance	Latched
Too High DC Offset	DC output voltage	Low	Output high impedance	Latched
Under Voltage on PVCC	PVCC < 4.5V	–	Output high impedance	Self-clearing
Over Voltage on PVCC	PVCC > 27V	–	Output high impedance	Self-clearing

DC DETECT PROTECTION

The TPA3131/32D2 has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the FAULT pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the DC Protection function to automatically drive the SDZ pin low which clears the DC Detect protection latch.

A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 60% for more than 420 msec at the same polarity. Table x below shows some examples of the typical DC Detect Protection threshold for several values of the supply voltage. This feature protects the speaker from large DC currents or AC currents less than 2Hz. To avoid nuisance faults due to the DC detect circuit, hold the SD pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

The minimum output offset voltages required to trigger the DC detect are show in Table 5. The outputs must remain at or above the voltage listed in the table for more than 420 msec to trigger the DC detect.

Table 5. DC Detect Threshold

PV_{CC} (V)	V_{OS} - OUTPUT OFFSET VOLTAGE (V)
4.5	0.96
6	1.30
12	2.60
18	3.90

SHORT-CIRCUIT PROTECTION AND AUTOMATIC RECOVERY FEATURE

The TPA3131/32D2 has protection from over current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULTZ pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SDZ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the short-circuit protection latch.

In systems where a possibility of a permanent short from the output to PVDD or to a high voltage battery like a car battery can occur, pull the MUTE pin low with the FAULTZ signal with a inverting transistor to ensure a high-Z restart, like shown in the figure below:

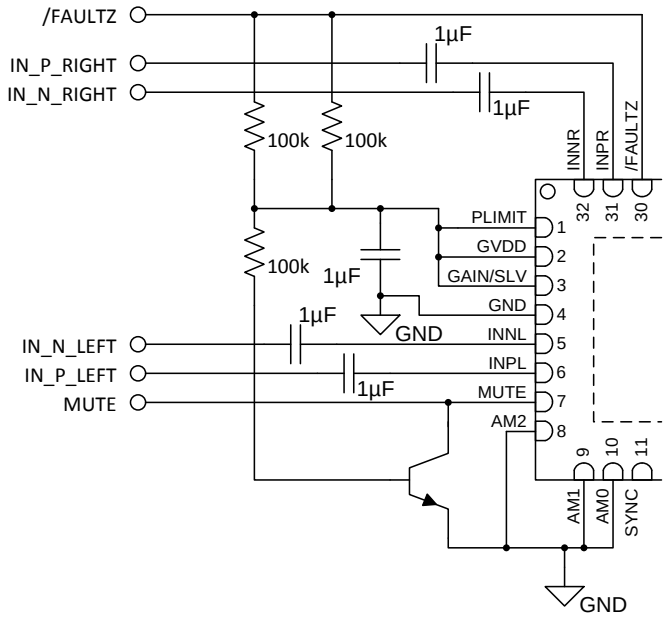


Figure 26. MUTE Driven by Inverted FAULTZ

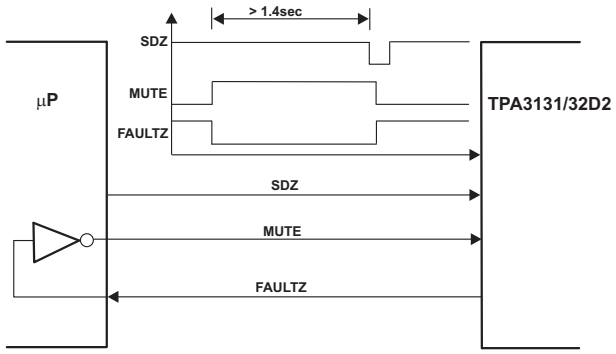


Figure 27. Timing Requirement for SDZ

THERMAL PROTECTION

Thermal protection on the TPA3131/32D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. This is a latched fault.

Thermal protection faults are reported on the FAULTZ terminal as a low state.

If automatic recovery from the thermal protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the thermal protection latch.

THERMAL DESIGN

Main thermal path for cooling the device is from the bottom side Power-Pad through multiple via connections in the PCB to the bottom side ground plane. The high power efficiency allows TPA3131D2 to be operated continuously at rated output power into both 4Ω and 8Ω load, and TPA3132D2 into 8Ω load using a PCB layout similar to what is used in the TPA3131D2/32D2 EVMs. The rated output power of TPA3132D2 into 4Ω load will be available only for a limited duration of time when using a PCB layout similar to the EVM layout. Sustained power output into 4Ω needs to be limited to prevent excess heating of the device. TPA3132D2 will be able to output full output power for a limited duration of time. The duration depends on the actual PCB layout. For the TPA3132D2 EVM layout the TPA3132D2 full output power with 4Ω load can be illustrated with a burst test at room temp (25°C):

Table 6. TPA3132D2 EVM Burst Output Power

BURST RATIO	FULL POWER 1kHz	REDUCED POWER 1kHz (1/8 of full power)	MAXIMUM DEVICE TEMPERATURE	PCB TEMPERATURE (Bottom Side, Under Device)
1:3	1 Cycle 44W/4Ω	2 Cycles 5.25W/4Ω	116°C	85°C
2:5	2 Cycles 44W/4Ω	3 Cycles 5.25W/4Ω	143°C	102°C

It is not recommended to operate the device with a maximum temperature above 150°C.

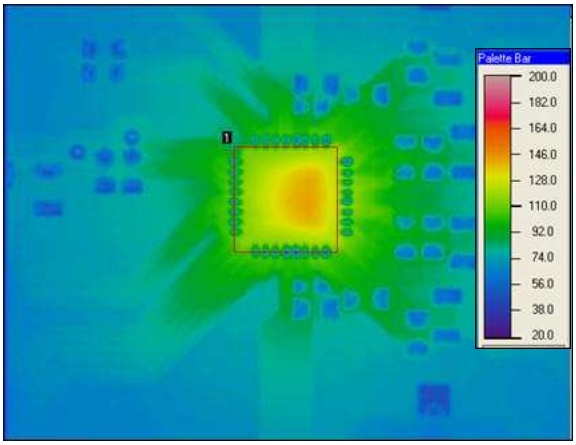


Figure 28. TPA3132D2 EVM TEMPERATURE WITH 2:5 (42W/5.25W/4Ω) BURST POWER

It is advised to use the PLIMT function to avoid thermal shutdown in system designs not using signal processing to limit the average output power. Such systems can accidentally exceed the thermal limits of the amplifier and a OTE shutdown will occur.

EFFICIENCY: LC FILTER REQUIRED WITH THE TRADITIONAL CLASS-D MODULATION SCHEME

The main reason that the traditional class-D amplifier-based on AD modulation needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 × VCC, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3131/32D2 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is VCC instead of 2 × VCC. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

FERRITE BEAD FILTER CONSIDERATIONS

Using the Advanced Emissions Suppression Technology in the TPA3131/32D2 amplifier it is possible to design a high efficiency class-D audio amplifier while minimizing interference to surrounding circuits. It is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter. One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30 MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. Examples of ferrite beads which have been tested and work well with the TPA3130D2 can be seen in the TPA3130D2EVM user guide SLOU341.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class-D outputs to ground. Suggested values for a simple RC series snubber network would be 18 Ω in series with a 330 pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the GND pins on the IC.

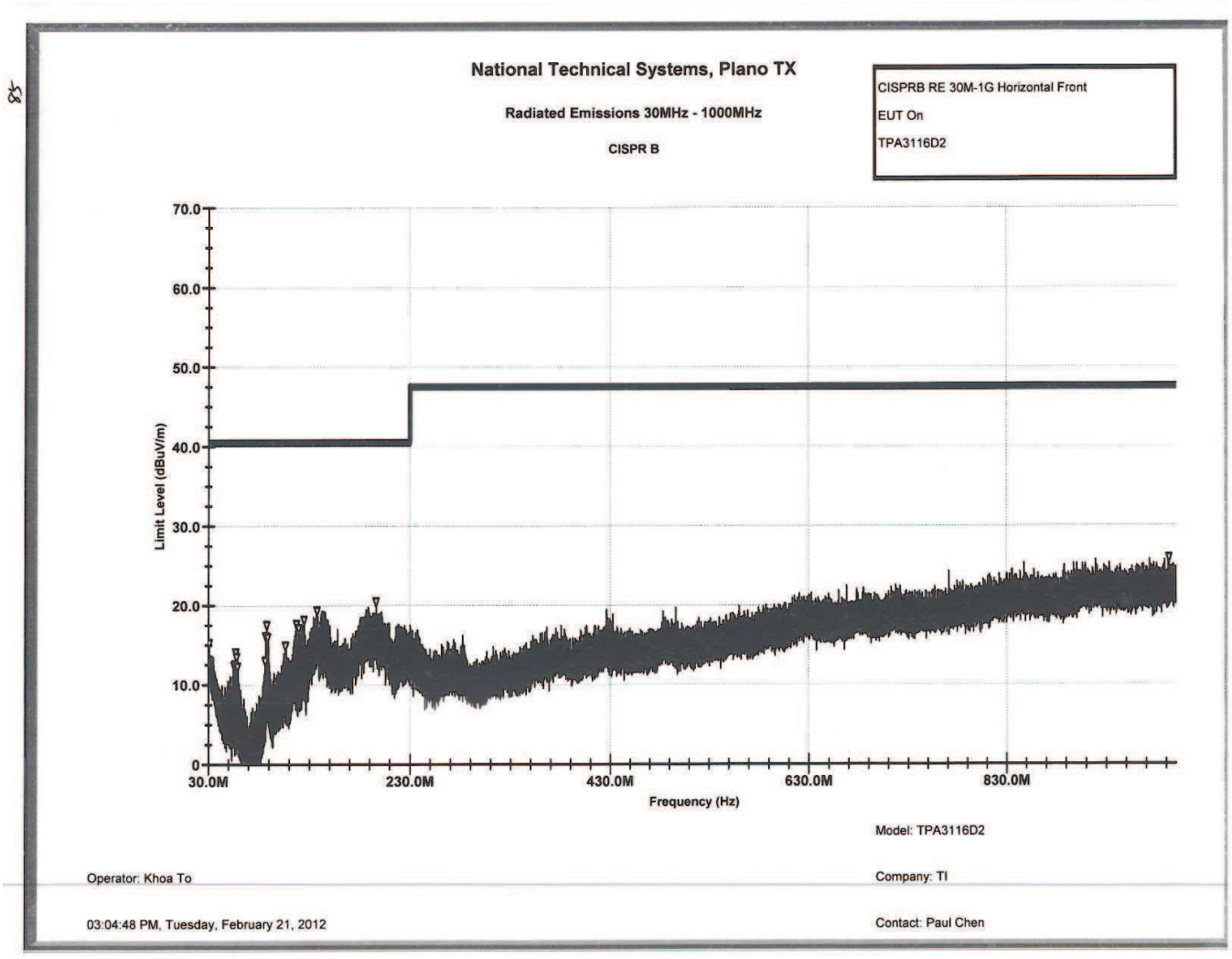


Figure 29.

WHEN TO USE AN OUTPUT FILTER FOR EMI SUPPRESSION

The TPA3131/32D2 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 125 cm and high power. The TPA3131/32D2 EVM passes FCC class-B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency.

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

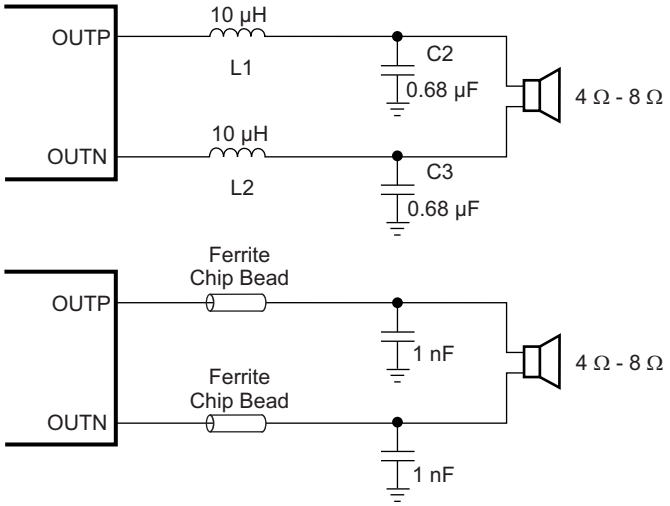


Figure 30.

AM AVOIDANCE EMI REDUCTION

To reduce interference in the AM radio band, the TPA3131/32D2 has the ability to change the switching frequency via AM<2:0> pins. The recommended frequencies are listed in Table 7. The fundamental frequency and its second harmonic straddle the AM radio band listed. This eliminates the tones that can be present due to the switching frequency being demodulated by the AM radio.

Table 7. AM Frequencies

US	EUROPEAN				
AM FREQUENCY (kHz)	AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)	AM2	AM1	AM0
	522-540				
540-917	540-914	500	0	0	1
917-1125	914-1122	600 (or 400)	0 0	1 0	0 0
1125-1375	1122-1373	500	0	0	1
1375-1547	1373-1548	600 (or 400)	0 0	1 0	0 0
1547-1700	1548-1701	600 (or 500)	0 0	1 0	0 1

PRINTED-CIRCUIT BOARD (PCB LAYOUT)

The TPA3131/32D2 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors — The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (100 µF or greater) bulk power supply decoupling capacitors should be placed near the TPA3131/32D2 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the IC GND pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1 nF and a larger mid-frequency cap of value between 100 nF and 1 µF also of good quality to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding — The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the TPA3131/32D2.
- Output filter — The ferrite EMI filter (see Figure 30) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded.

For an example layout, see the TPA3131/32D2 Evaluation Module (TPA3131/32D2EVM) User Manual. Both the EVM user manual and the thermal pad application report are available on the TI Web site at http://www.ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA3131D2RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3131	Samples
TPA3131D2RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3131	Samples
TPA3132D2RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3132	Samples
TPA3132D2RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3132	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

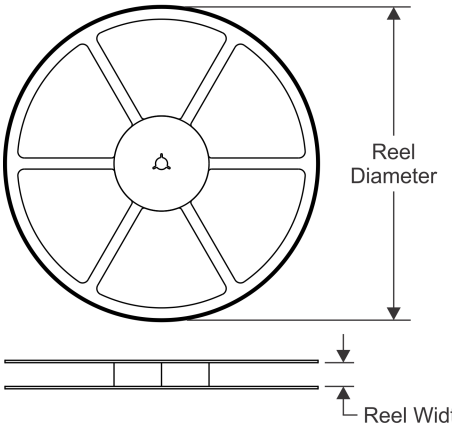
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

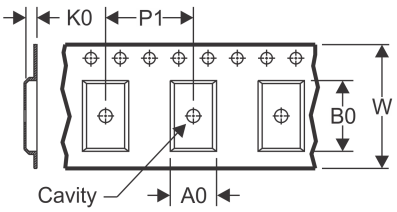
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

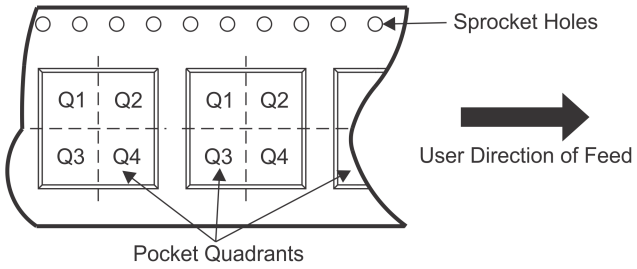


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

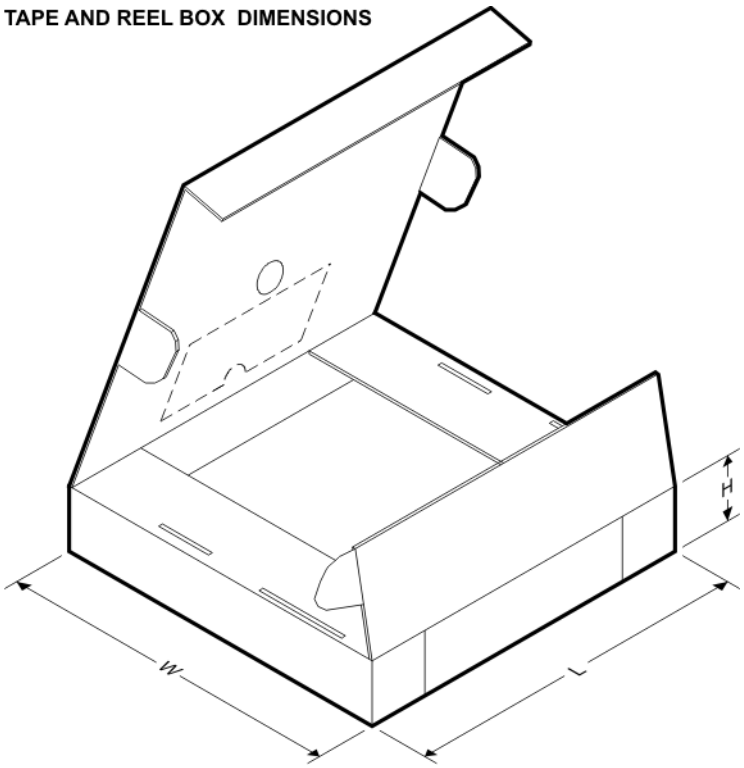
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3131D2RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPA3131D2RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPA3132D2RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPA3132D2RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

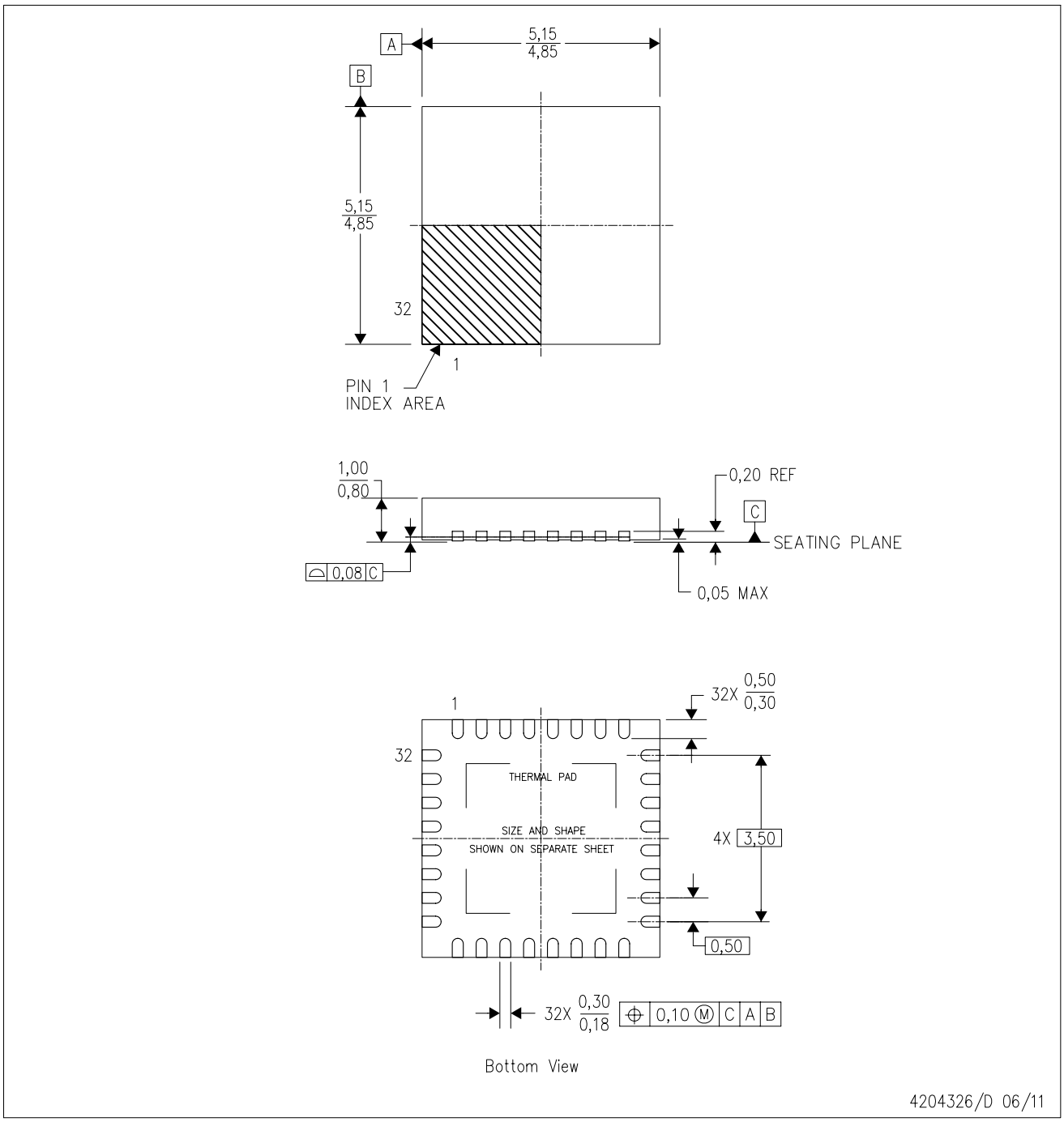
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3131D2RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TPA3131D2RHBT	VQFN	RHB	32	250	210.0	185.0	35.0
TPA3132D2RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TPA3132D2RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

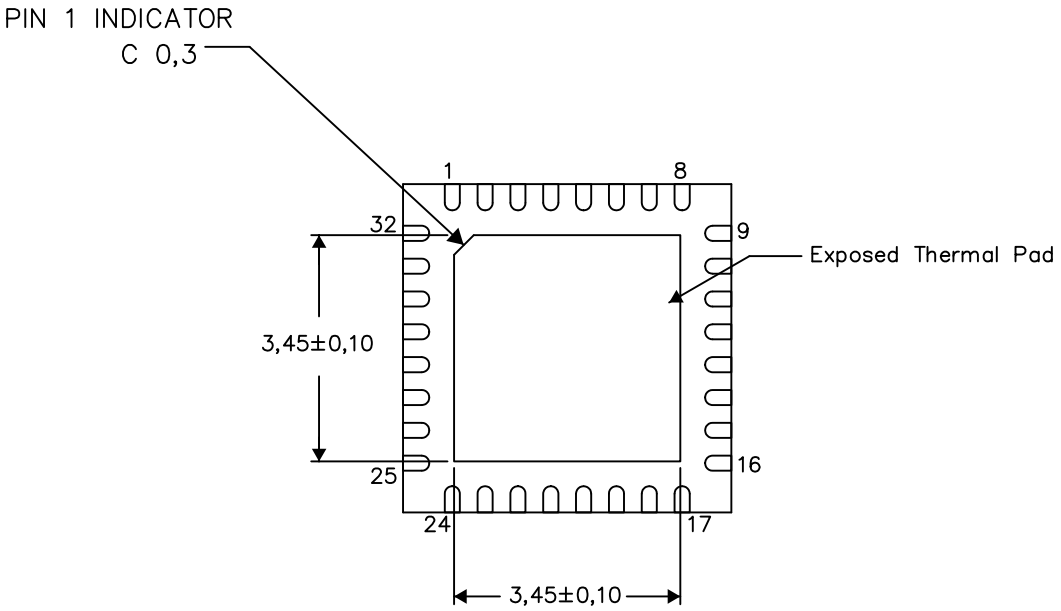
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



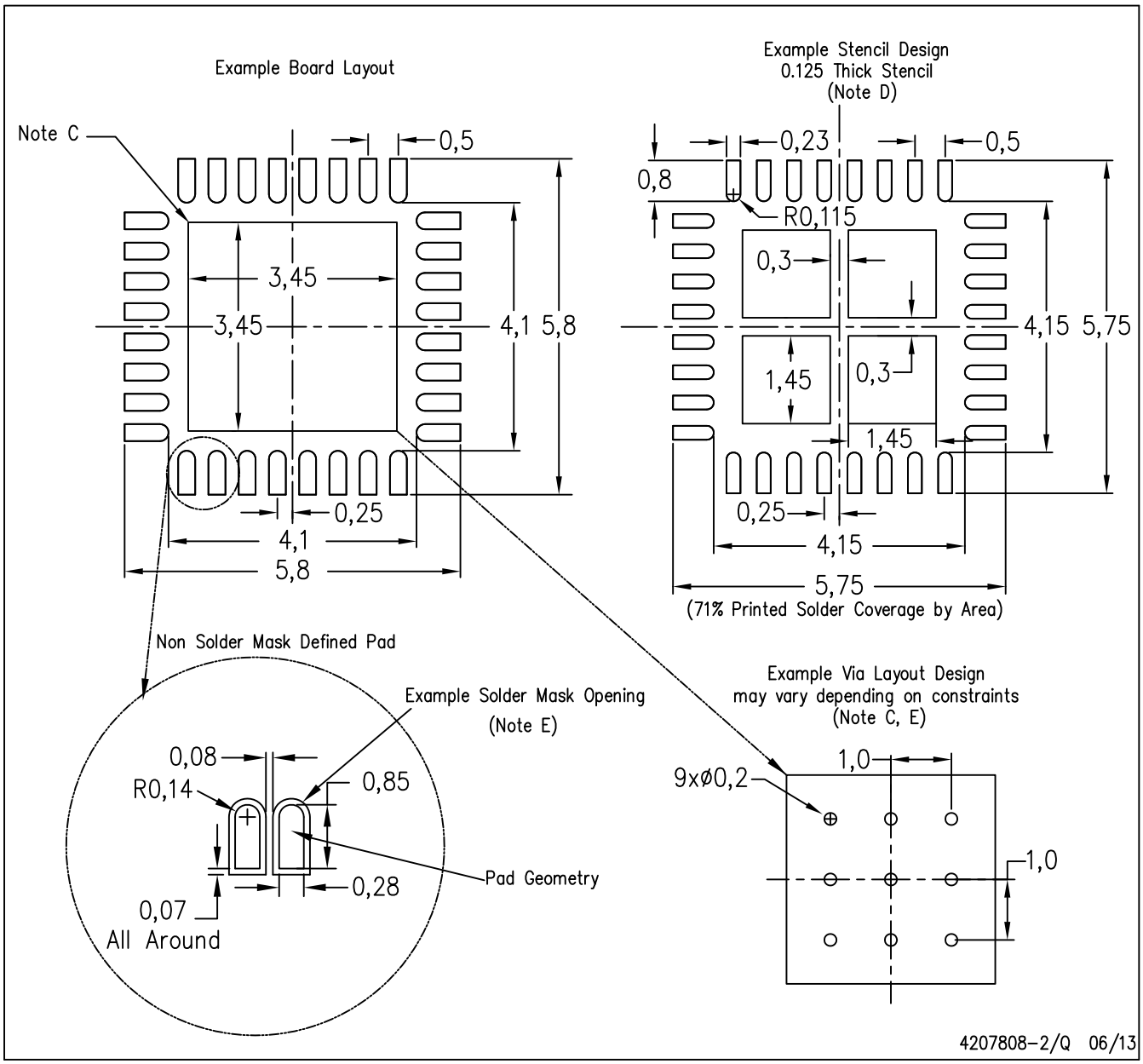
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/Y 06/13

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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