## AM4915P

## **Analog Power**

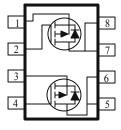
# Dual P-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low  $r_{DS(on)}$  assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low r<sub>DS(on)</sub> Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Extended VGs range (±25) for battery pack applications

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$r_{DS(on)} m(\Omega) = I_D($			
-30	$17.5 @ V_{GS} = -10V$	-9.5		
	$23 @ V_{GS} = -4.5V$	-8.5		





ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter		Symbol	Maximum	Units		
Drain-Source Voltage		$V_{DS}$	-30	V		
Gate-Source Voltage		V <sub>GS</sub>	±25	v		
Continuous Drain Current <sup>a</sup>	$T_A=25^{\circ}C$	I.	-9.5			
Continuous Drain Current	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	ID	-8.2	А		
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	±50			
Continuous Source Current (Diode Conduction) <sup>a</sup>		Is	-2.1	Α		
	$T_A=25^{\circ}C$	D <sub>n</sub>	2.0	W		
Power Dissipation <sup>a</sup>	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	гD	1.3			
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Maximum	Units		
Maximum Junction-to-Case <sup>a</sup>	t <= 5 sec	$R_{\theta JC}$	40	°C/W		
Maximum Junction-to-Ambient <sup>a</sup>	t <= 5 sec	$R_{\theta JA}$	78	°C/W		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

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<b>D</b>			Limits			TT *4	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Drain-Source Breakdown Voltage	V(BR)DSS	$V_{GS} = 0 V$ , $I_D = -250 uA$	-30			v	
Gate-Threshold Voltage	VGS(th)	$V_{DS} = V_{GS}, I_D = -250 \text{ uA}$		-1.6	-3	v	
Gate-Body Leakage	Igss	$V_{DS} = 0 V, V_{GS} = \pm 25 V$			±100	nA	
Zana Cata Valta ao Drain Currant	I	$V_{DS} = -24 V, V_{GS} = 0 V$			-1		
Zero Gate Voltage Drain Current	Idss	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^{\circ}\text{C}$			-5	uA	
On-State Drain Current <sup>A</sup>	ID(on)	$V_{DS} = -5 V, V_{GS} = -10 V$	-50			Α	
	ĨDS(on)	$V_{GS} = -10 \text{ V}, I_D = -11.5 \text{ A}$		15.5	17.5	mΩ	
Drain-Source On-Resistance <sup>A</sup>		$V_{GS} = -4.5 \text{ V}, I_D = -9.3 \text{ A}$		20.5	23		
		$V_{GS} = -10 V$ , $I_D = -13 A$ , $TJ = 55^{\circ}C$		16.5	22		
Forward Tranconductance <sup>A</sup>	gfs	$V_{DS} = -15 V$ , $I_D = -11.5 A$		29		S	
Diode Forward Voltage	Vsd	$I_{S} = 2.5 A, V_{GS} = 0 V$		-0.8	-1.2	V	
Dynamic <sup>b</sup>							
Total Gate Charge	Qg	$V_{DS} = -15 V$ , $V_{GS} = -10 V$ , $I_D = -11.5 A$		64	100	nC	
Gate-Source Charge	Qgs			11			
Gate-Drain Charge	Qgd			17			
Switching	· · · · ·						
Turn-On Delay Time	td(on)	$V_{DD} = -15 \text{ V}, \text{ R}_{L} = 6 \Omega$ , $\text{ID} = -1 \text{ A},$		15	25	nS	
Rise Time	tr			13	20		
Turn-Off Delay Time	td(off)	VGEN = -10 V		100	152		
Fall-Time	tf			54	81		

Notes

a. Pulse test:  $PW \le 300$  us duty cycle  $\le 2\%$ .

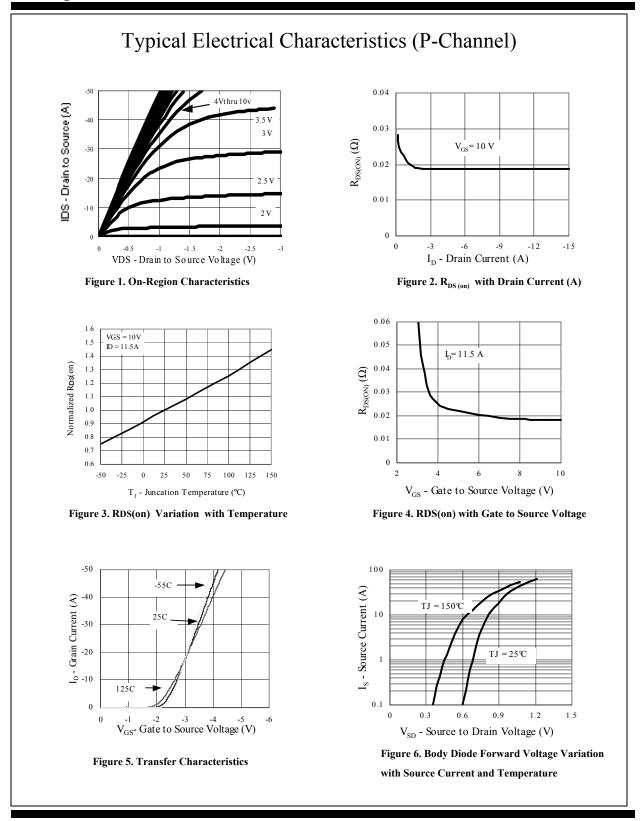
b. Guaranteed by design, not subject to production testing.

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